

Product Specification

Model Name	S024HQ56NN
Description	Standard LCD Module 2.4 " WQVGA 240 (RGB)x 320 Dots
Date	2024/4/17
Version	1.0

Approved by/Date	Check by/Date	Prepared by/Date
HL 2024/4/17	HXY 2024/4/17	MHY 2024/4/17

Customer Approval	
Date	

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2023-6-29	First Release.	MHY
	2024-4-17	Update color green X value	MHY

2. General Specifications

Feature		Spec
Characteristics	Size	2.4 inch
	Resolution	240 (horizontal)* 320 (Vertical)
	Interface	RGB/MCU
	Connect type	Connector
	Display Colors	262K
	Technology type	a-Si
	Pixel pitch (mm)	0.153 * 0.153
	Pixel Configuration	R.G.B-Stripe
	Display Mode	Normally Black
	LCD Driver IC	ILI9341V
	Viewing Direction	Full view
Mechanical	LCM (W x H x D) (mm)	42.72 * 59.46 * 2.00
	Active Area(mm)	36.72 * 48.96
	Weight (g)	TBD
	LED Numbers	4 LEDs

Note 1: Requirements on Environmental Protection: RoHs

Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

LCD PIN-MAP

No.	Symbol	Description																																												
1	NC	No connection																																												
2	IM0	<table><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80-16bit parallel I/F</td><td>DB[15:0]</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-9bit parallel I/F</td><td>DB[8:0]</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-18bit parallel I/F</td><td>DB[17:0],</td></tr><tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr><tr><td>2 data lane serial I/F</td><td>SDA: in/out WRX: in</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr></table>	IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	0	80-8bit parallel I/F	DB[7:0]	0	0	0	1	80-16bit parallel I/F	DB[15:0]	0	0	1	0	80-9bit parallel I/F	DB[8:0]	0	0	1	1	80-18bit parallel I/F	DB[17:0],	0	1	0	1	3-line 9bit serial I/F	SDA: in/out	2 data lane serial I/F	SDA: in/out WRX: in	0	1	1	0	4-line 8bit serial I/F	SDA: in/out
IM3	IM2		IM1	IM0	MPU Interface Mode	Data pin																																								
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0	0		0	1	80-16bit parallel I/F	DB[15:0]																																								
0	0		1	0	80-9bit parallel I/F	DB[8:0]																																								
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		2 data lane serial I/F			SDA: in/out WRX: in																																									
0	1	1	0	4-line 8bit serial I/F	SDA: in/out																																									
3	IM1																																													
4	IM2																																													
5	IM3																																													
6	RESET	Global reset pin																																												
7	VSYNC	Vertical sync input. Negative polarity																																												
8	HSYNS	Horizontal sync input. Negative polarity																																												
9	DOTCLK	Dot-clock signal and oscillator source																																												
10	DE	Data enable input. Active high to enable the input data bus under “DE Mode”																																												
11-28	DB17-DB0	Data bus																																												
29	SDO	Serial data output																																												
30	SDI	Serial data input																																												
31	RD	Read signal																																												
32	RS/SCL	Serial data select/Serial clock signal																																												
33	WR	Write signal																																												
34	CS	Chip select input signal																																												
35	FMARK	TE																																												
36	VCC	Power supply																																												
37	VCC	Power supply																																												
38	GND	Ground																																												
39	GND	Ground																																												
40	LEDA	Power for LED backlight (Anode)																																												
41	LEDK	Power for LED backlight (Cathode)																																												
42	NC(XR)	No connection																																												
43	NC(YD)	No connection																																												
44	NC(XL)	No connection																																												
45	NC(YU)	No connection																																												

4. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	VDD	-0.5	-	5	V	-
Operating Temperature	TOPR	-20	-	70	°C	-
Storage Temperature	TSTG	-30	-	80	°C	

5. Electrical Characteristics

5.1 Driving TFT LCD Panel

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Signal Voltage	Low Level	VIL	VDD	-	0.3*VDD	V	
	High Level	VIH	0.7*VDD	-	VDD	V	
Module Main Voltage		+3.3_VDD_TFT	3.0	3.3	3.6	V	
Module Main Current		+3.3_IDD_TFT	8.0	12.0	16.0	mA	
Module Main Power		+3.3_PDD_TFT	0.0240	0.0396	0.0576	W	

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	-	20	-	mA	
Forward Voltage	VF	10.8	-	13.6	V	
Backlight Power consumption	WBL	0.216	-	0.272	W	
LED Life-time	N/A	-	30000	-	Hrs	

Note 1: Each LED: IF =20 mA, VF =3.2+/-0.2V.

Note 2: Optical performance should be evaluated at Ta=25°C only.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

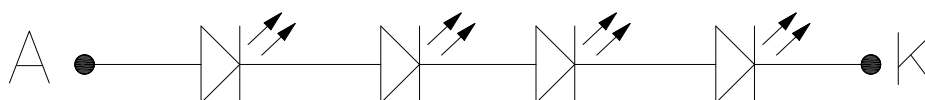
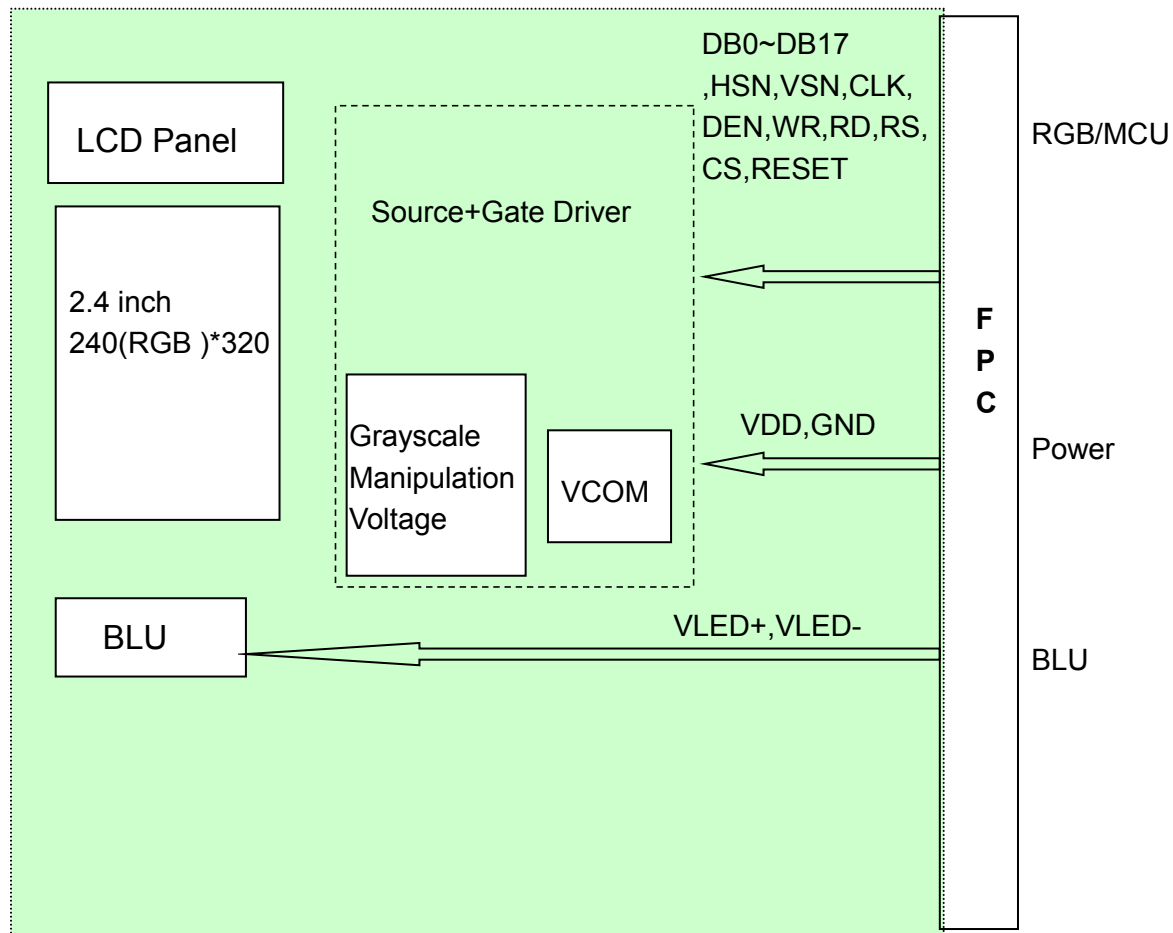


Figure: LED connection of backlight(Constant Current)

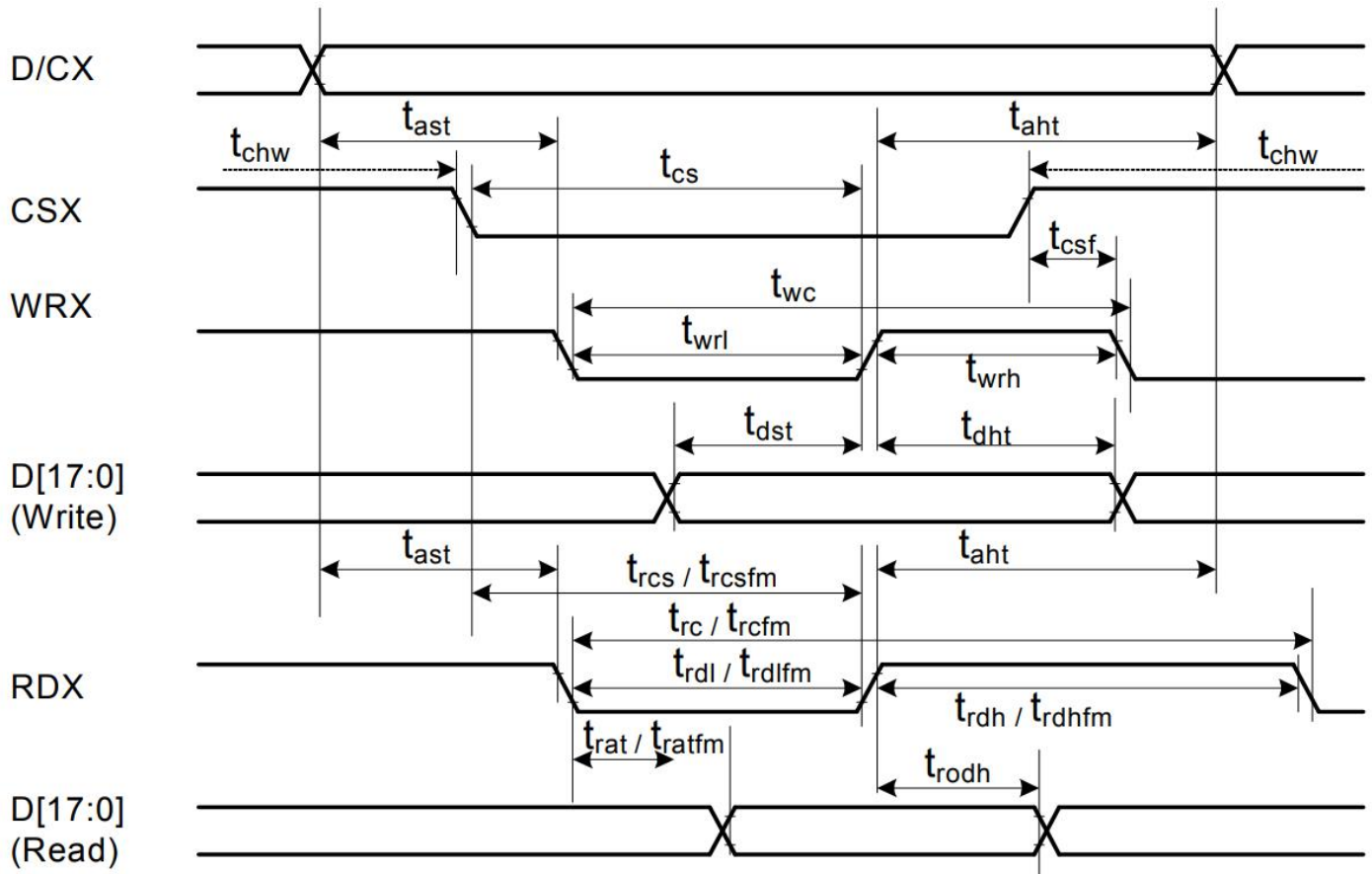
5.3 Block Diagram



6. Interface Timing

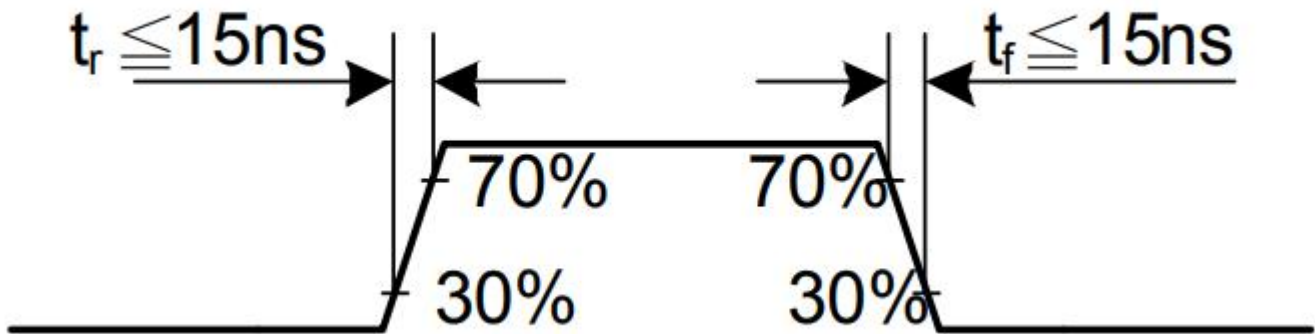
6.1 Timing Parameter

6.1.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-II system)

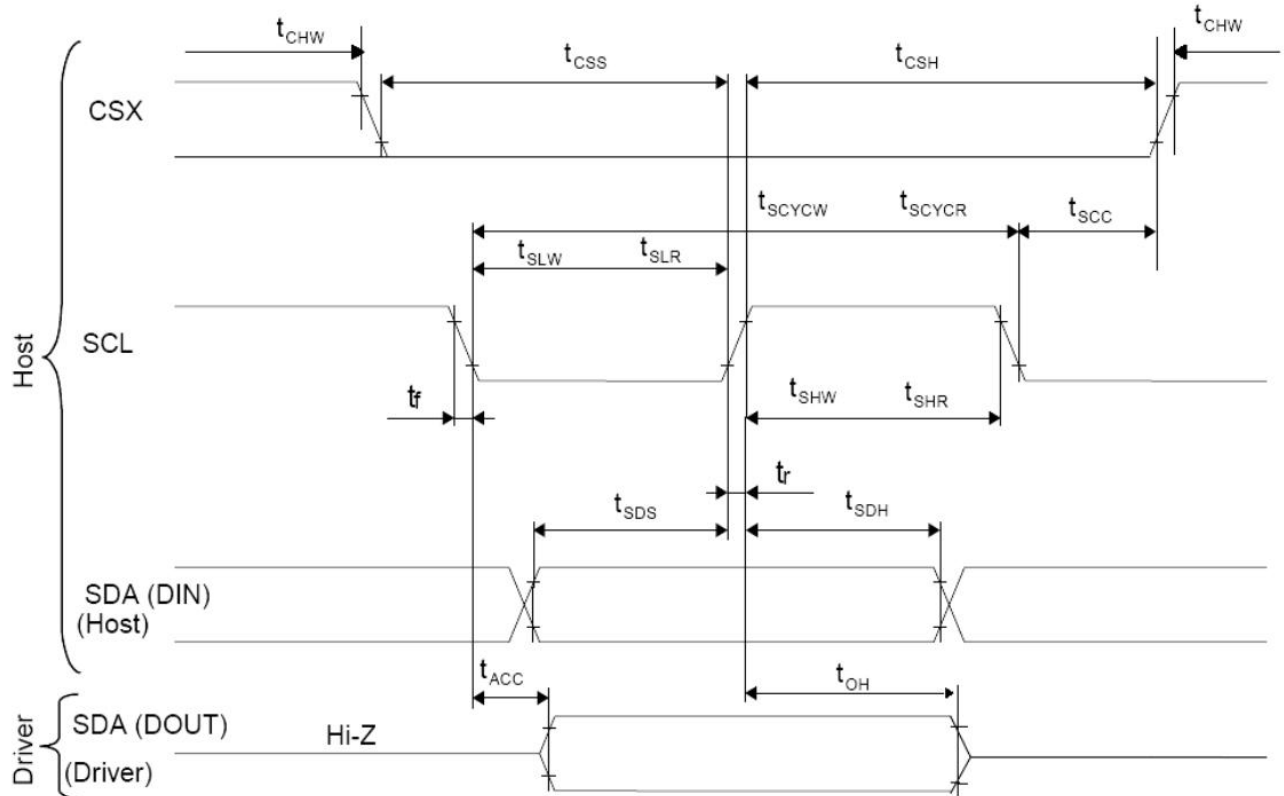


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchwh	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



6.1.2 Display Serial Interface Timing Characteristics (3-line SPI system)

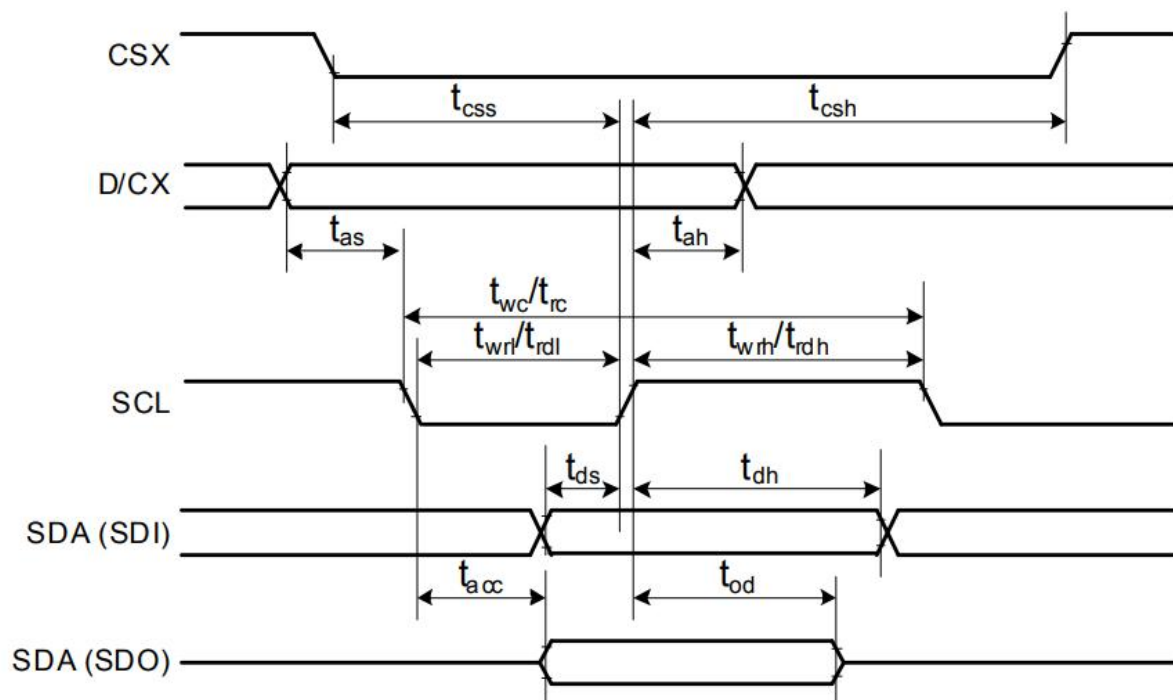


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: $T_a = 25^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

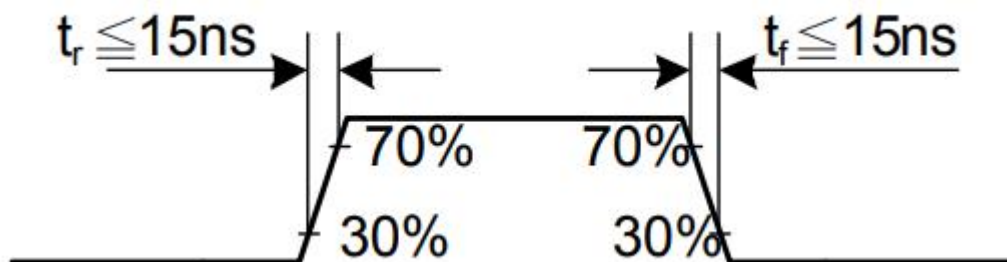


6.1.3 Display Serial Interface Timing Characteristics (4-line SPI system)

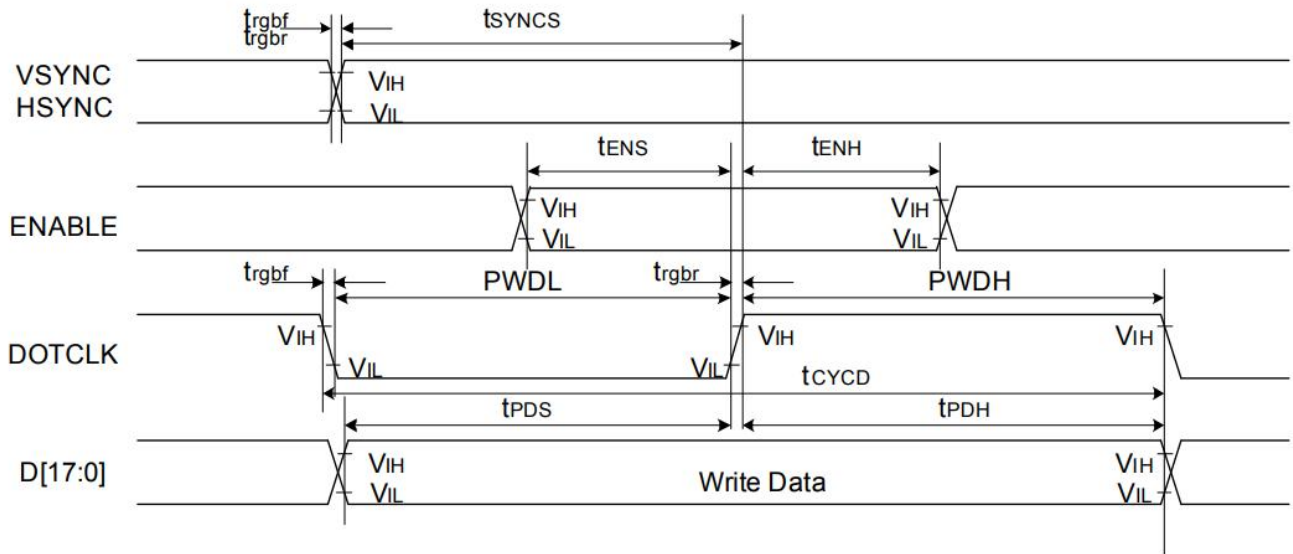


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Read)	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	40	-	ns	
	t_{wrh}	SCL "L" pulse width (Write)	40	-	ns	
	t_{trc}	Serial clock cycle (Read)	150	-	ns	
	t_{trdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{trdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-		
	t_{ah}	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{acc}	Access time (Read)	10	-	ns	For maximum CL=30pF
	t_{od}	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: $T_a = 25^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

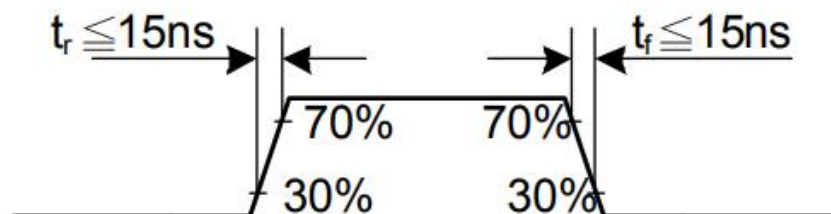


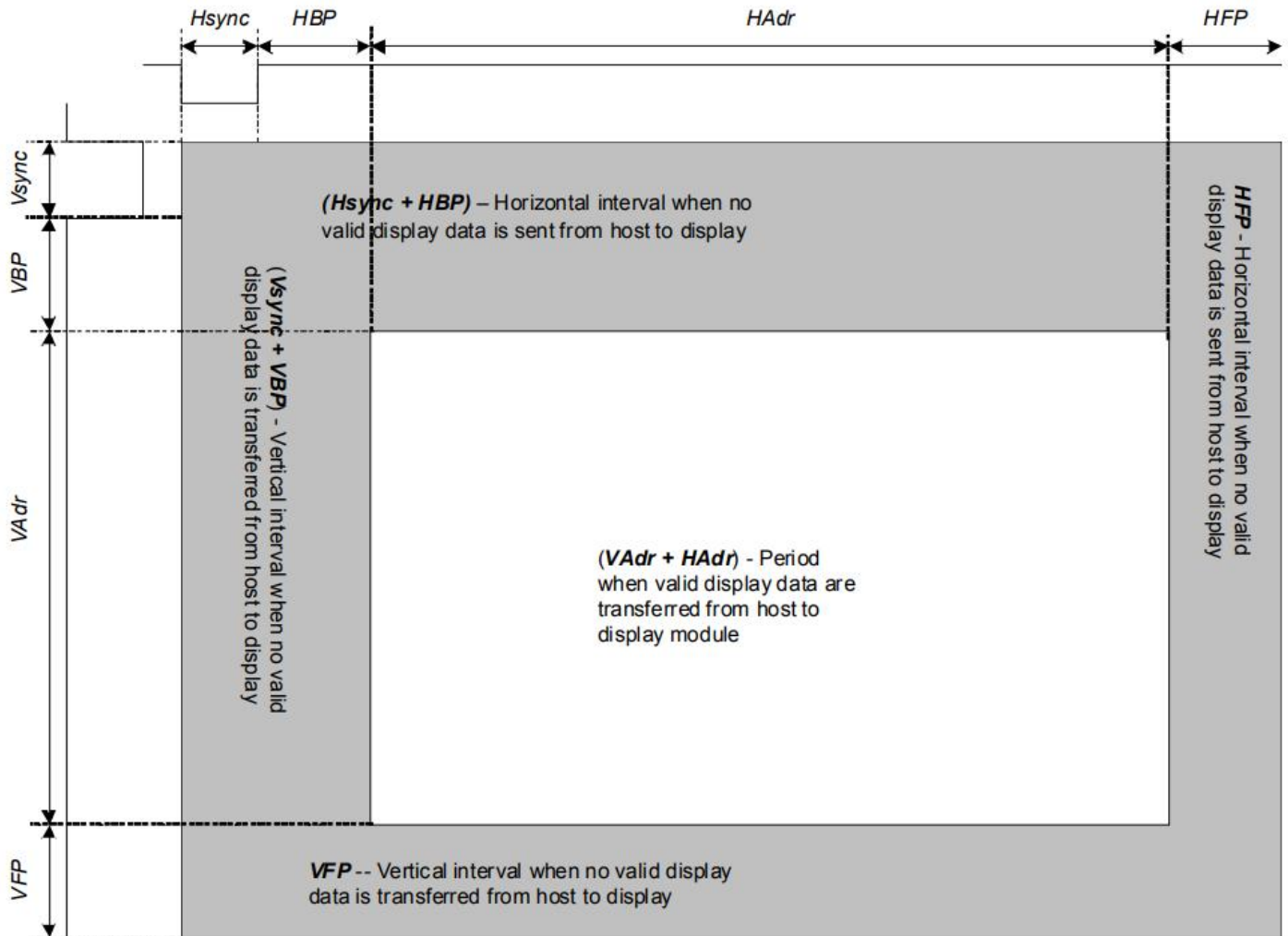
6.1.4 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgb}, t_{rgb}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgb}, t_{rgb}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70°C , $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{CI}=2.5\text{V}$ to 3.3V , $AGND=VSS=0\text{V}$

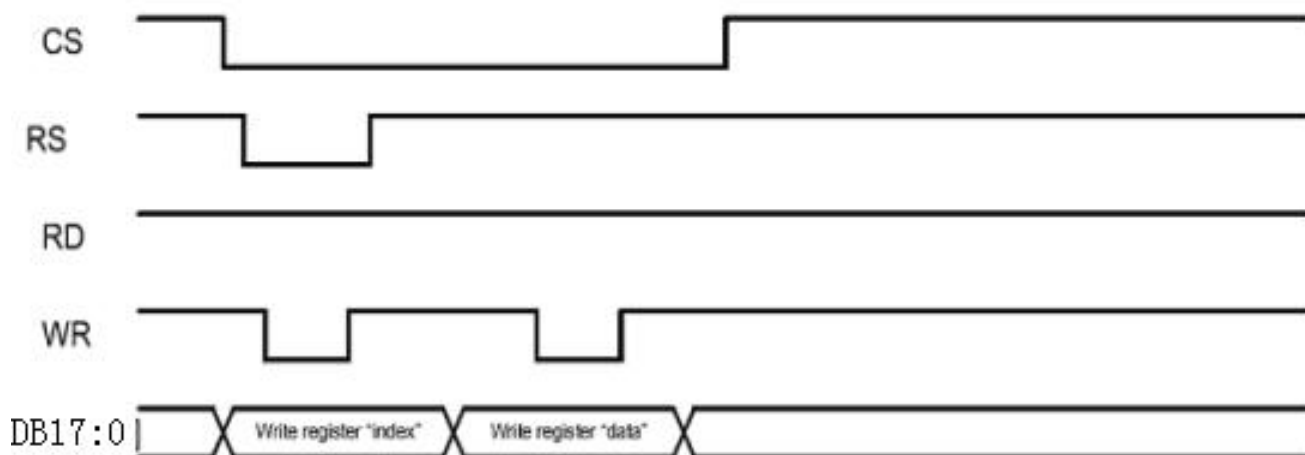




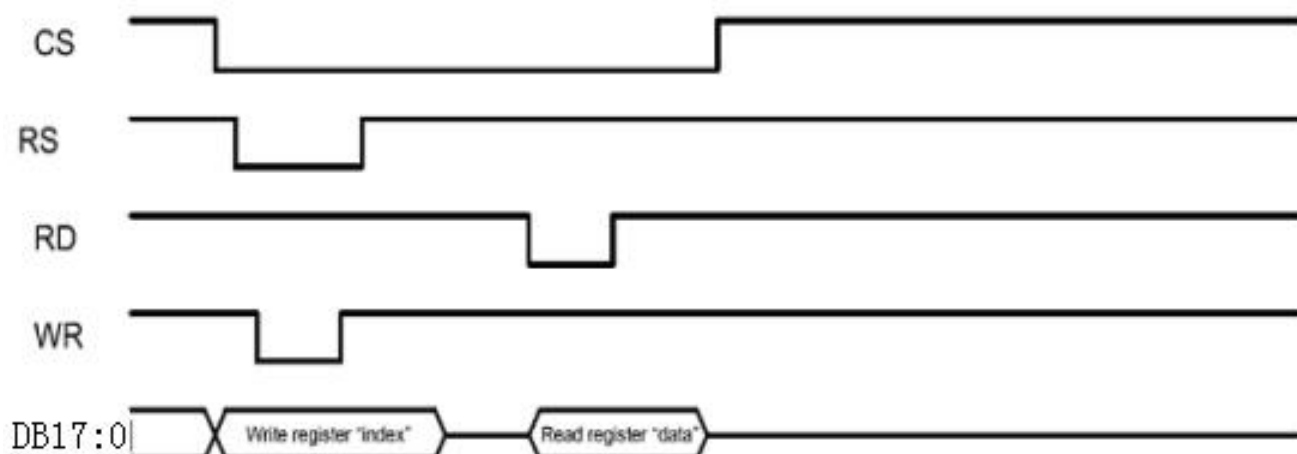
Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

6.2 Register White/Read Timing

(a) Write to register

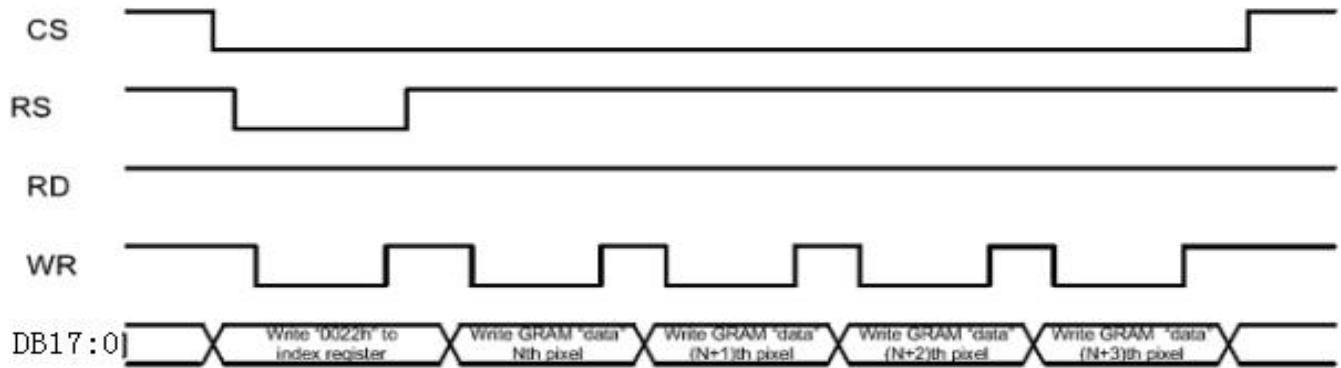


(b) Read from register

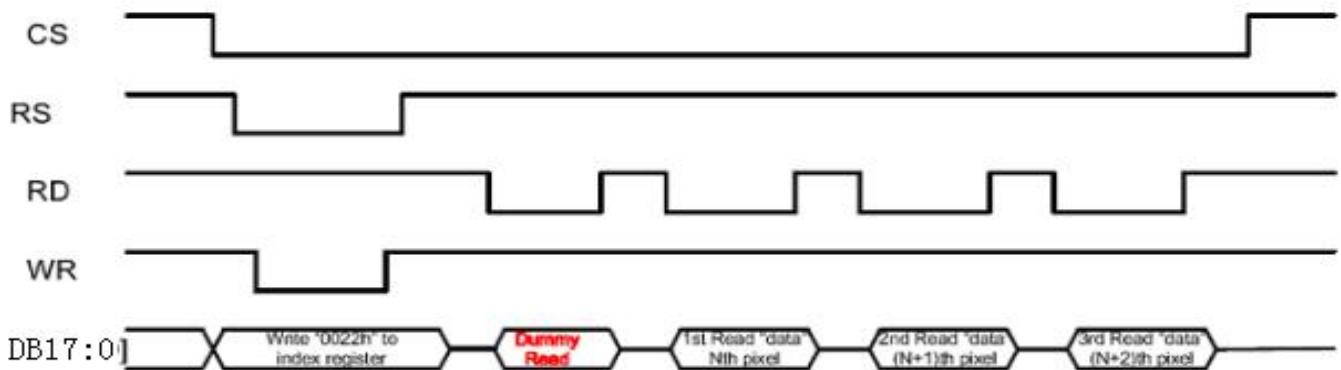


6.3 GRAM White/Read Timing

(a) Write to GRAM

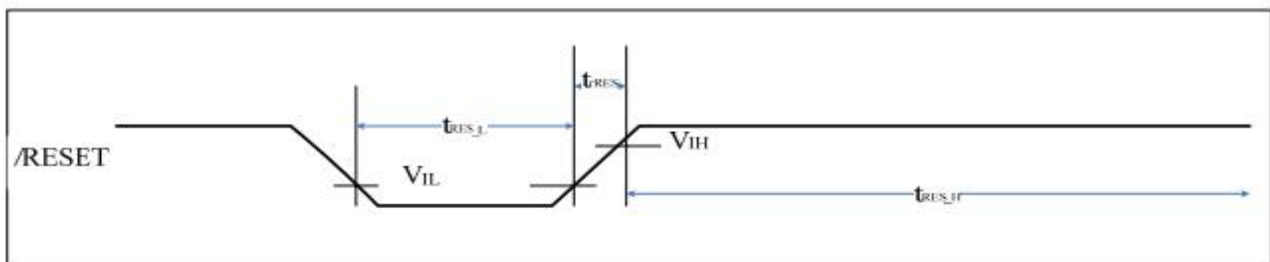


(b) Read from GRAM



6.4 Reset Timing Characteristics

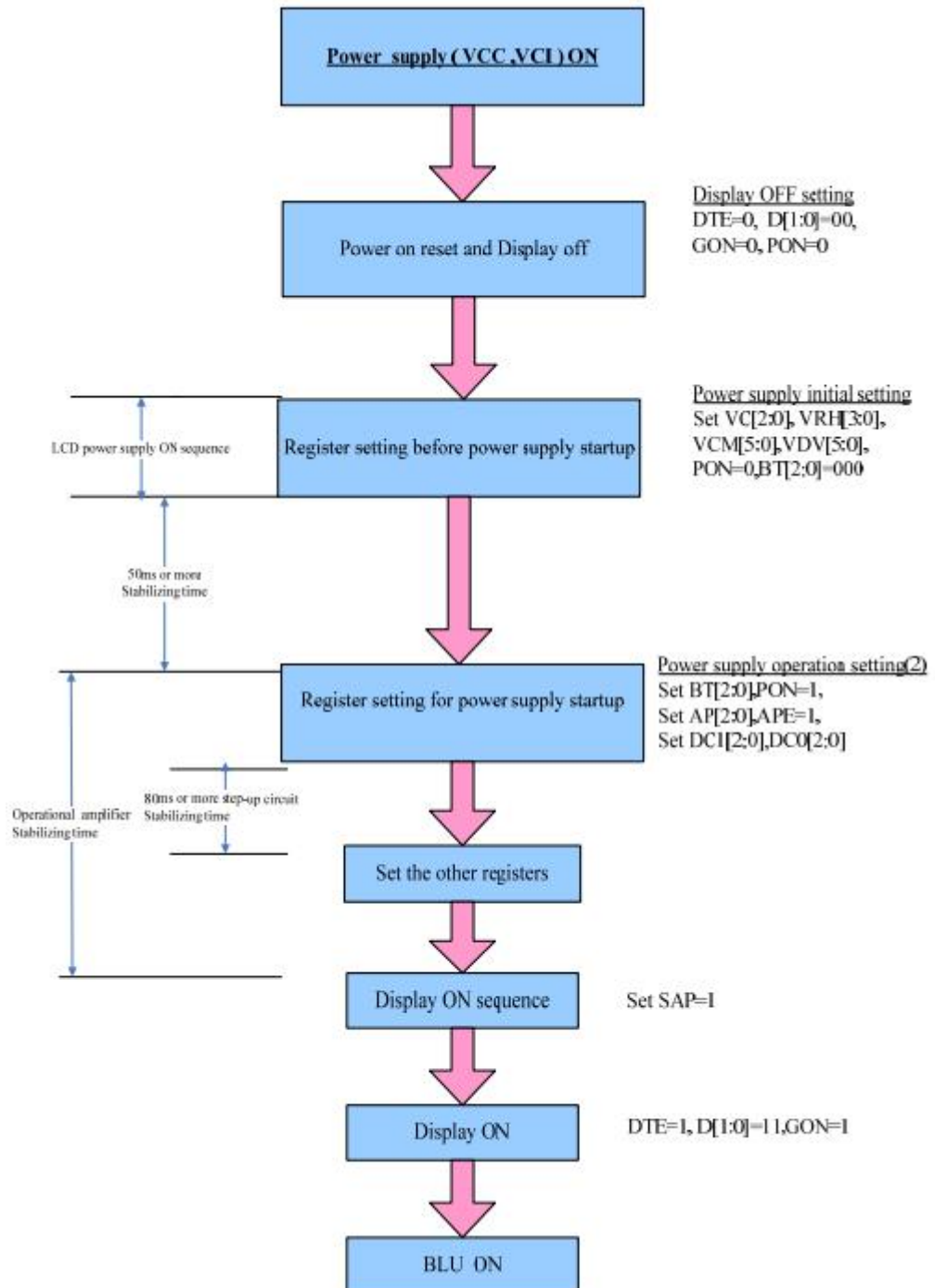
Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RESL}	ms	1	-	-
Reset rise time	t_{RES}	μs	-	-	10
Reset high-level width	t_{RESH}	ms	50		



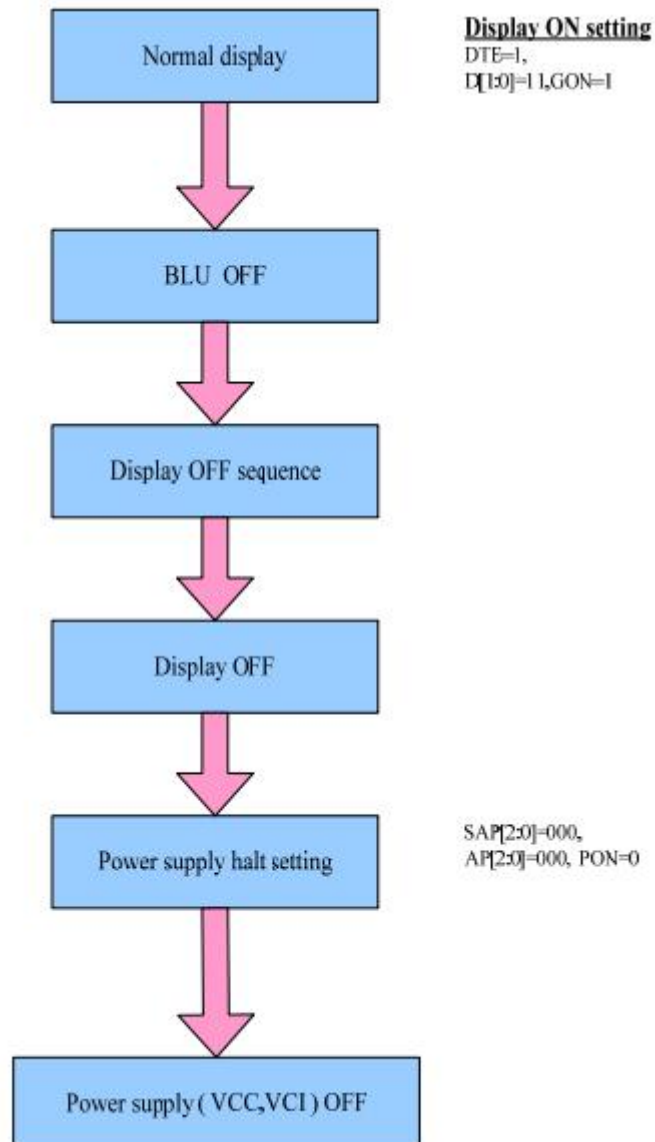
Reset timing

6.5 Power On/Off Sequence

6.5.1 Power On Sequence



6.5.2 Power Off Sequence



7. Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		T _{ON}	-	-	16	21	ms	FIG.1	Note4
		T _{OFF}		-	19	24			
Contrast Ratio		CR	-	640	800	-	-	FIG.2	Note1
Surface luminance		LV	$\theta = 0^\circ$	170	220	-	cd/m ²	FIG.2	Note2
Luminance uniformity		Y _U	$\theta = 0^\circ$	75	80	-	%	FIG.2	Note3
NTSC		-	$\theta = 0^\circ$	-	70	-	%	FIG.2	Note5
Viewing angle		θ_T	Center CR $\geq$ 10	-	80	-	deg	FIG.3	Note6
		θ_B		-	80	-	deg	FIG.3	
		θ_L		-	80	-	deg	FIG.3	
		θ_R		-	80	-	deg	FIG.3	
Chromaticity	Red	R _X	$\theta = 0^\circ$ $\phi = 0^\circ$ Ta=25°	0.597	0.647	0.697	-	FIG.2 CIE1931	Note5
		R _Y		0.267	0.317	0.367	-		
	Green	G _X		0.285	0.335	0.385	-		
		G _Y		0.532	0.582	0.632	-		
	Blue	B _X		0.090	0.140	0.190	-		
		B _Y		0.038	0.088	0.138	-		
	White	W _X		0.260	0.310	0.360	-		
		W _Y		0.286	0.336	0.386	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is based on TOPCON's BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3,,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (Tr) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Tf) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is based on Autronic-Melchers's ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

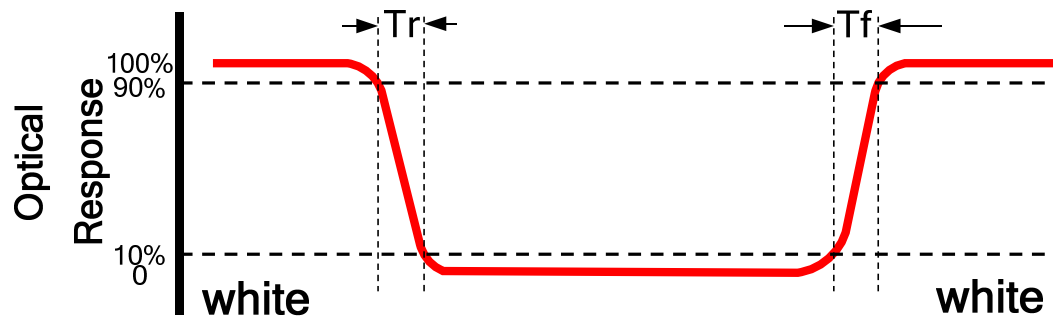


FIG.2. Measuring method for contrast ratio, surface luminance,

luminance uniformity, CIE (x,y) chromaticity

Size : $S \leq 5"$ (see Figure a) A : 5 mm B : 5 mm

H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

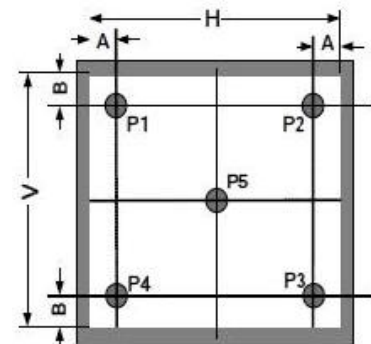


Figure a

Size : $5" < S \leq 12.3"$ (see Figure b) H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

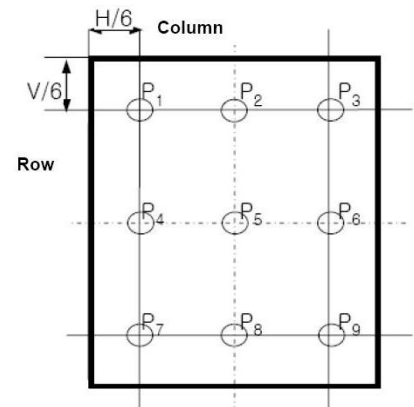


Figure b

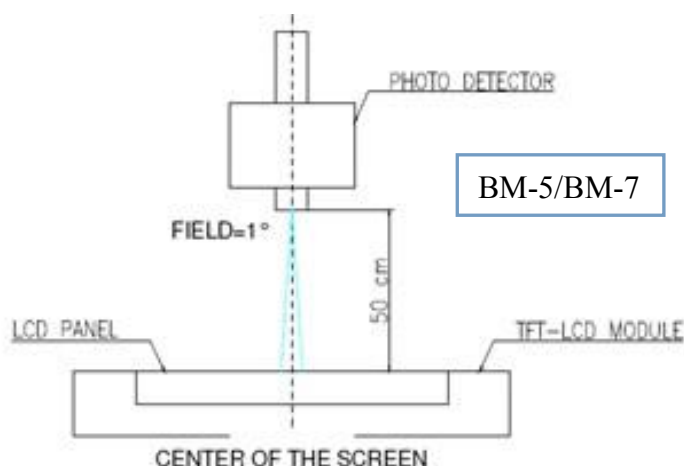
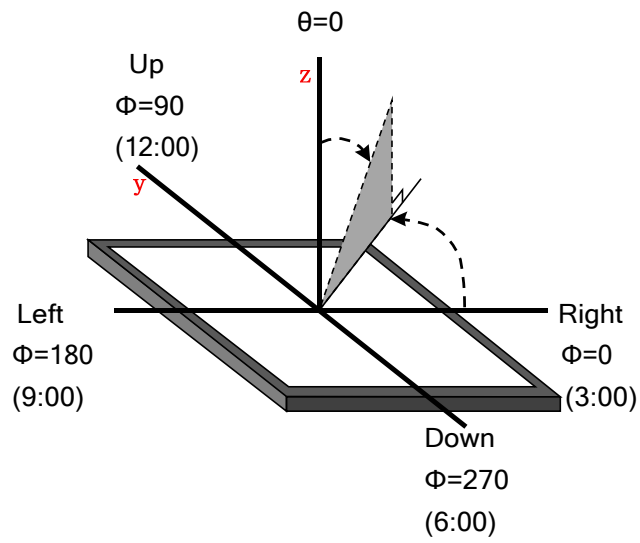


Figure c

FIG.3.The definition of viewing angle



8. Environmental / Reliability Tests

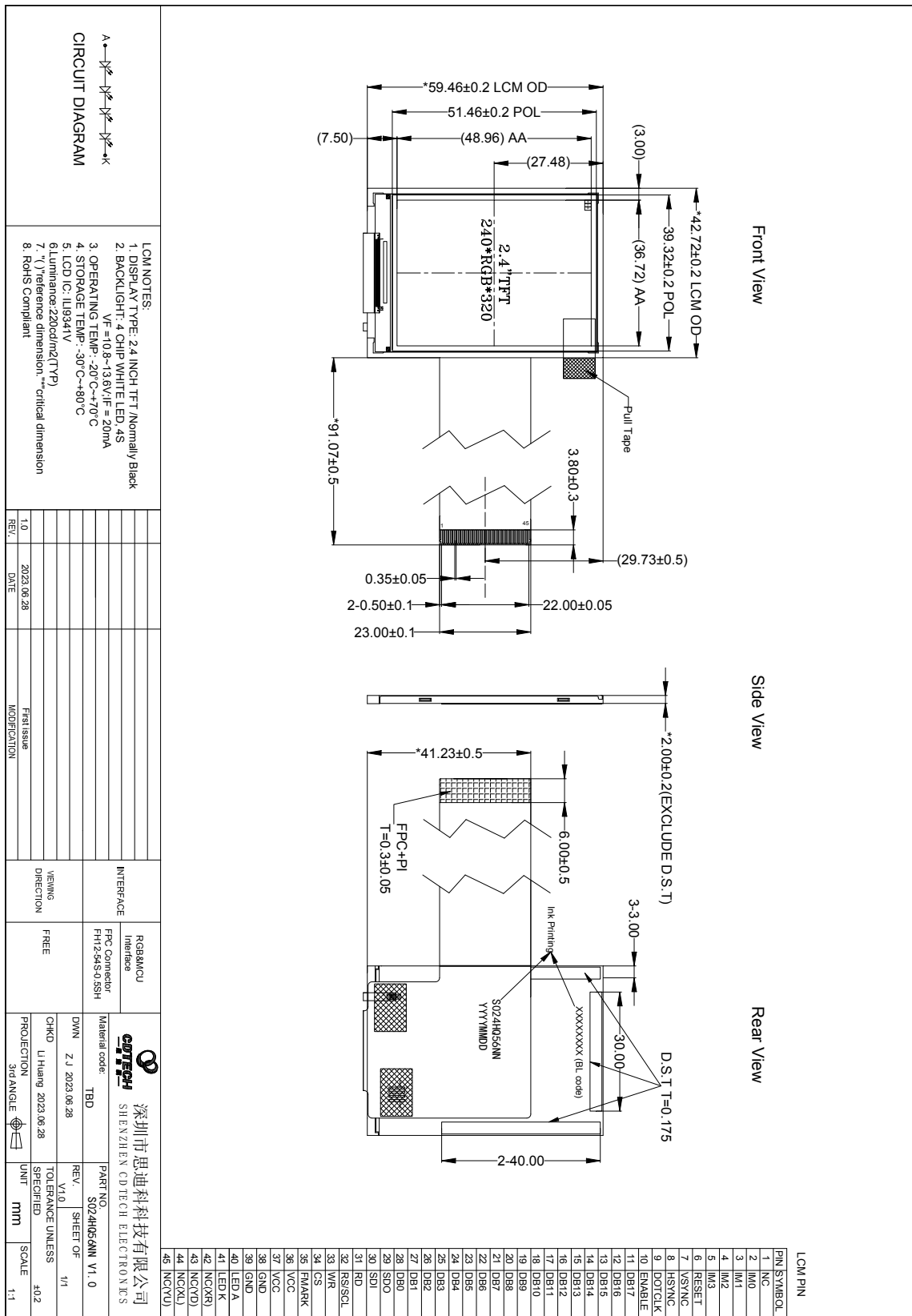
No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423.2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 96hrs	IEC60068-2-2 GB2423.2-89
4	Low Temperature Storage	Ta= -30℃, 96hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 96 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air: ±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. Ts is the temperature of panel's surface.

2. Ta is the ambient temperature of sample.

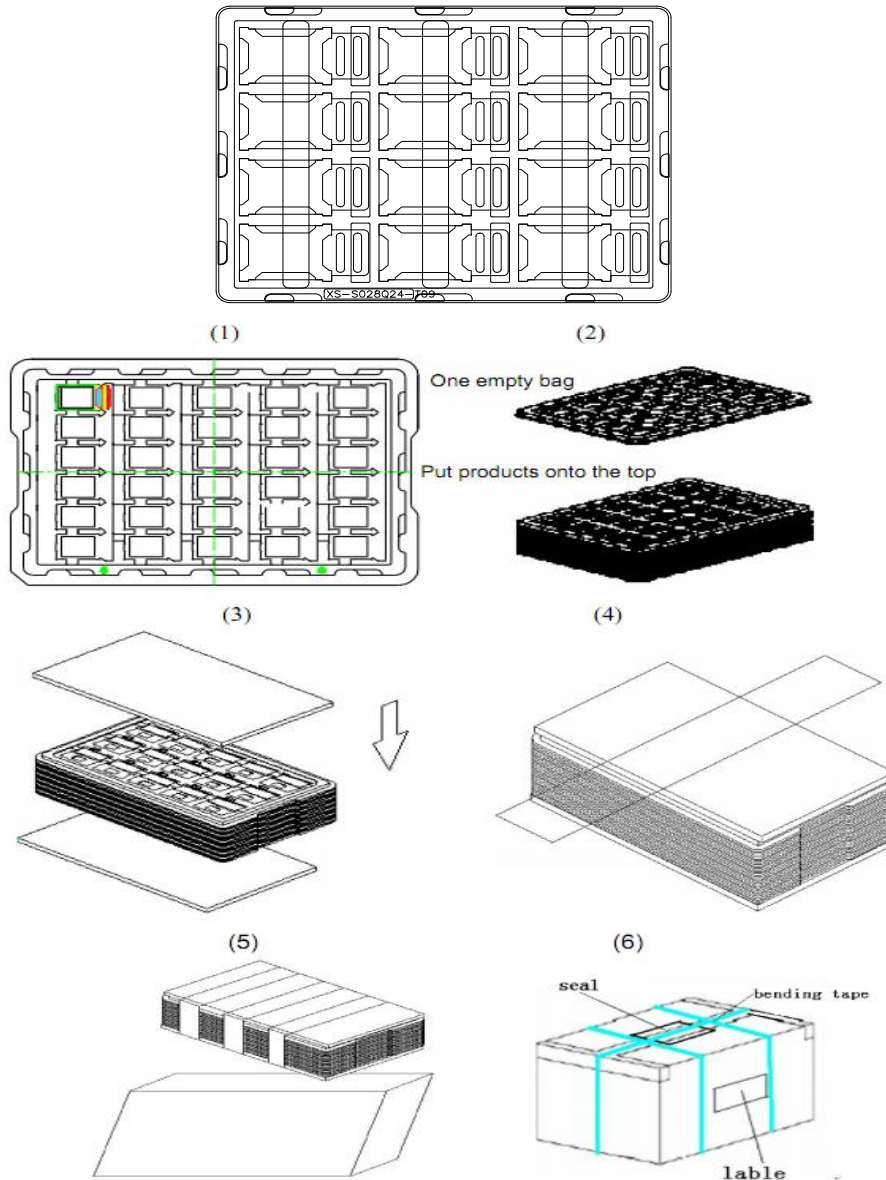
3. The size of sample is 5pcs.

9. Mechanical Drawing



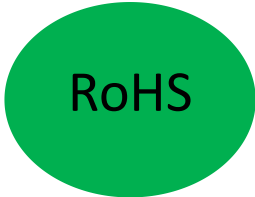
10. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

Three Five Corp.			
产品描述 Description	2.4" LCD module		
产品型号 Part No.	TFC-D9240RTQV25-C1A		
客户料号 Customer P/N			
参考号 Reference No.			
原产地 Country of origin	CHINA	生产批号 Lot No.	
净重 Net weight		毛重 Gross weight	
数量 Quantity		生产日期 Date	

11. TFT-LCD Module Inspection Criteria

11.1 Objective

The TFT criteria is set to formalize the TFT quality standards with reference to customer for inspection.

11.2 Scope

The criteria is applicable to all TFT products (Include TFT , TFT+RTP or TFT+CTP) manufactured by TFC.

11.3 Tools for Inspection

Tester, calipers, multi-meter, anti-static wrist straps, finger cots, desk Lamps, etc.

11.4 Sampling Plan and Reference Standards

11.4.1 Sampling plan:

Refer to GB/T2828.1-2012/ISO2859-1:1999 //MIL-STD-105E

AQL: level II; normal:

1) MA=0.40

2) MI=0.65

11.4.2 IPC-A-610 Acceptability of Electronic Assemblies.

11.5 Inspection Conditions and Inspection Reference

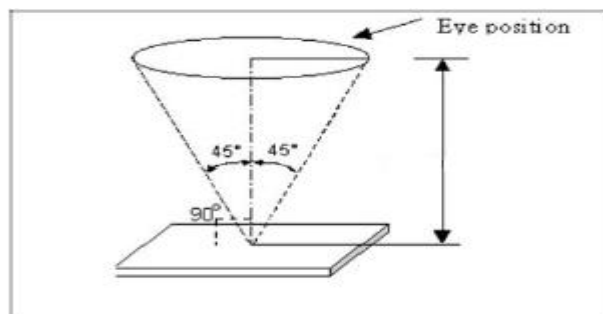
11.5.1 Cosmetic inspection with naked eyes:

1) Temperature: $23 \pm 5^{\circ}\text{C}$; relative humidity: 45~75%RH

2) Illumination: 500lux~1000lux

3) Distance: $30\text{cm} \pm 5$ from the inspector's naked eyes to the LCD panel.

4) View angle: within 45° from perpendicular to LCM surface (view direction and special parameters refer to production specification).



11.5.2 Definition

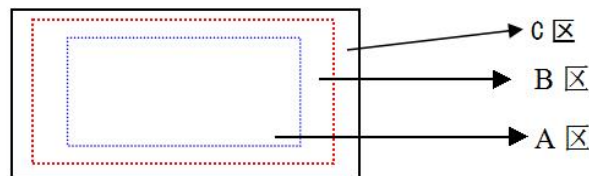
11.5.2.1 Area definition

A area: Active area (AA area)

B area: Viewing area (VA area)

C area: non-view area (out of B area)

11.5.2.2 Any cosmetic defect which do not affect product quality and customer assembling in C area, it's Acceptable. (The dimension is defined on the drawings)



11.5.2.3 Test condition: refer to product specification

11.5.3 Defect type:

11.5.3.1 A area defect type:

Line defect (scratch, soft flocks, fibre)、dot defect (white dot, black dot, same color dot, different color dot, bubble), stain, pin-hole, light leak, scratch.

11.5.3.2 B area defect type:

Broken, crack/chipping, FPC defect

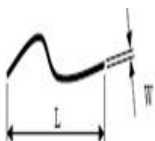
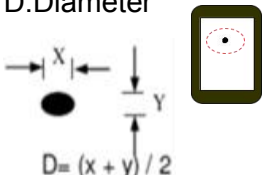
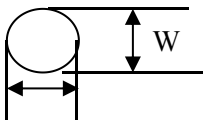
11.5.3.3 Undefined items or other special items, refer to mutual agreement and limited sample by customer.

11.5.3.4 Test condition: refer to product specification.

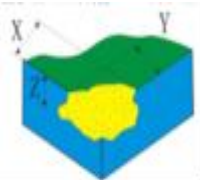
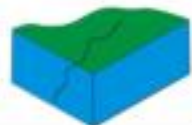
11.6.Defects and Acceptance Standards

11.6.1 Appearance inspection

11.6.1.1 Dot/line defect

Defect	S < 5"	Accepted standard	MAJ	MIN
S/C , line defect W:width L:length 	$W \leq 0.03\text{mm}$	Accept		√
	$0.03\text{mm} < W \leq 0.10\text{mm}$, $L \leq 5\text{mm}$ quantity ≤ 2 distance $> 10\text{mm}$	Accept		√
	$W > 0.10\text{mm}$ $L > 5\text{mm}$	Reject		√
Dot defect (black/white spot, foreign objects etc) D:Diameter 	$D \leq 0.10\text{mm}$	Accept		√
	$0.10\text{mm} < D \leq 0.25\text{mm}$ quantity ≤ 2 distance $> 10\text{mm}$	Accept		√
	$D > 0.25\text{mm}$	Reject		√
Polarizer with air bubble, convex-concave dots or dent defect  $d = (w + l) / 2$	$D \leq 0.20\text{mm}$	Accept		√
	$0.20\text{mm} < D \leq 0.5\text{mm}$ quantity ≤ 2	Accept		√
	$d > 0.5\text{mm}$	Reject		√

11.6.1.2 Chip and Crack

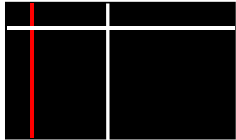
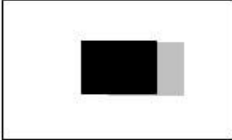
Defect	S < 5"	Accepted standard	MAJ	MIN
Chip 	$X \leq 0.3\text{mm}$, $Y \leq 0.3\text{mm}$, one side ≤ 1	Accept		√
	$X > 0.3\text{mm}$, $Y > 0.3\text{mm}$	Reject		√
Sensor chip	Not affect ITO line, not lengthen, function test is OK. And be non-visual after attaching Lens.	Accept		√
	Affect ITO line and be visual.	Reject		√
Glass crack 	Glass crack.	Reject		√

11.6.1.3 Attaching defect (kapton tape/protective film)

Defect	Description	Accepted standard	MAJ	MIN
High temperature kapton tape	Kapton tape attached on FPC doesn't meet the criterion of drawing.	Reject		√
Protective film	Clean、attaching flat、no shifting	Accept		√

11.6.2 TFT defects and Inspection Criterion

11.6.2.1 Function items

Defects	Inspection Criterion	Pictures	Inspection method/tools	Defect category
No display /function	shows no picture/display in normal connected situation. ->Rejected		Naked eyes/ testers	MA
Missing segment	Shows missing lines in normal display.->Rejected		Naked eyes/ testers	MA
Image retention (sticking)	The previous picture stays in the next picture. Disappear time <10s, OK; time>10s, NG		Naked eyes/ testers	MA
Flicker	Not accepted	/	Naked eyes/ testers	MA
Display abnormal	Not accepted		Naked eyes/ testers	MA
Display dim/bright	Refer to bright value definition	/	Naked eyes/ BM-7	MA
Contrast	Refer to SPEC	/	Naked eyes/ BM-7	MA
White/ black dot White/ black speckle	Refer to dot criterion	/	Naked eyes	MI

11.6.1.2 LCD pixel defect(defect category: MI)

Item	Accepted
Size	S <5"
Pixel defect (RGB dot)	1
2 connected bright pixel dot	0
3 connected bright pixel dot or more	0
Bright pixel dot quantity	1
Random dark pixel dot quantity	2
2 connected dark pixel dot	1
3 connected dark pixel dot or more	0
Dark pixel dot quantity	3
Multi-bright pixel dot	ND 5 % hidden, OK
<p>Remark: 2 bright pixel dots distance $DS \geq 15mm$ 2 dark pixel dots distance $DS \geq 5mm$</p> <p>1) Bright pixel dot: Power on TFT and RGB dot in black display</p> <p>2) Dark pixel dot: Power on TFT and gray or black dot in RGB display</p> <p>3) Multi-bright pixel dot: Power on TFT and fluorescent tiny dot in black display(only visible in black display)</p>	

11.7 Others

11.7.1 Some defect items are not defined in this document, obey to final agreement between customer and manufacturer or sign limit sample.

11.7.2 If final goods include FPC/PCB, inspection criterion refers to IPC-610, Level 2.

12. Precautions for Use of LCD modules

12.1 Handling Precautions

12.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

12.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

12.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

12.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

12.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

12.1.6 Do not attempt to disassemble the LCD Module.

12.1.7 If the logic circuit power is off, do not apply the input signals.

12.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

12.1.8.1 Be sure to ground the body when handling the LCD Modules.

12.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

12.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

12.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

12.2 Storage Precautions

12.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

12.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

12.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

12.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.