CDTech(H.K.)Electronics Limited

Product Specification

Model Name	S035GQ11NS
Description	TFT LCD Module 3.5" QVGA 320(RGB)x240 Dots
Date	2018/12/06
Version	1.0

Approved by/Date	**Check by/Date**	**Prepared by/Date**
ZHP 2018/12/06	HZX 2018/12/06	Yigui.Han 2018/12/06

Customer Approval	
Date	

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2018/12/06	First release.	Yigui.Han

2. General Specifications

Feature		Spec
Characteristics	Size	3.5 inch
	Resolution	320(horizontal)*240(Vertical)
	Interface	1. 8/ 9/ 16/ 18-bit 6800-series / 8080-series Parallel Interface 2. Serial Peripheral Interface (SPI) 3. 18-/6-bit RGB interface (DEN, DOTCLK,HSYNC,VSYNC,DB[17:0]) 4. VSYNC interface (system interface + VSYNC) 5. WSYNC interface (system interface + WSYNC)
	Connect type	Connector
	Color Depth	262K
	Technology type	a-Si
	Pixel pitch (mm)	0.219 x 0.219
	Pixel Configuration	R.G.B.-Stripe
	Display Mode	Normally White
	Driver IC	SSD2119
	Viewing Direction	12 O'clock
	Gray Inversion Direction	6 O'clock
Mechanical	LCM (W x H x D) (mm)	76.84*63.84*3.27
	Active Area(mm)	70.08 x 52.56
	With/Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	6 LEDs

Note 1: Requirements on Environmental Protection: RoHs
Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

LCD PIN-MAP

No.	Symbol	Description
1	VCI	Booster input voltage pin
2	VCI	Booster input voltage pin
3	VSS	Ground
4	VDDIO	Voltage input pin for logic
5	VSS	Ground
6	RESET	Reset Signal pin (“Low” is enable)
7	DC/SDC(RS)	Data or Command select PIN.
8	E/RD	6800 system: E(enable signal) 8080 system : RD(read strobe signal) Serial mode: Not use and should be connected to VDDIO or VSS
9	WR	6800 system : RW (indicates read cycle when high ,write cycle when low) 8080 system : WR (write strobe signal)
10	CS	Chip select
11	SCL	Serial Clock.
12	SD0	Serial Data output
13	SDI	Serial Data Input
14	WSYNC	Ram write synchronization output. Leave it OPEN when not used.
15~32	D17~D0	Data bus
33	VSS	Ground
34	DOTCLK	Dot-clock signal and oscillator source
35	HSYNC	Line Synchronous Signal
36	VSYNC	Frame Synchronous Signal
37	DE	Display enable pin for controller
38	VSS	Ground
39	PS0	Interface select PIN
40	PS1	
41	PS2	
42	PS3	
43	VSS	Ground
44~47	NC	NC
48	VSS	Ground
49	LEDK	Backlight LED Cathode
50	LEDA	Backlight LED Anode.

PS3	PS2	PS1	PS0	Interface Mode	Data bus input
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]
0	0	0	1	8-bit 6800 parallel interface	D[17:10]
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]
0	0	1	1	8-bit 8080 parallel interface	D[17:10]
0	1	0	0	9-bit generic D[9:16] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally	
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI	
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI	
0	1	1	1	6-bit generic D[8:3] (262k colour) + 3-wire SPI	
1	0	0	0	18-bits 6800 parallel interface	D[17:0]
1	0	0	1	9-bits 6800 parallel interface	D[17:9]
1	0	1	0	18-bit 8080 parallel interface	D[17:0]
1	0	1	1	9-bit 8080 parallel interface	D[17:9]
1	1	1	0	3-wire SPI	
1	1	1	1	4-wire SPI	

4. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	V_{DD}	-0.3	-	5.0	V	-
Operating Temperature	T_{OPR}	-20	-	70	℃	-
Storage Temperature	T_{STG}	-30	-	80	℃	

5. Electrical characteristics

5.1 Driving TFT LCD Panel

Items	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply voltage	VCI	2.5	3.3	3.6	V	
Power supply pin of IO pins	VDDIO	1.4	3.3	3.6	V	
Current consumption	IVCI+IVDDIO	-	-	10	mA	NOTE
Dot Clock	DCK	-	5.5	8.2	MHz	

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	
Forward Voltage	V_F	18	19.2	20.4	V	
Backlight Power consumption	W_{BL}	-	0.384	-	W	
LED Lifetime		-	30000	-	Hrs	

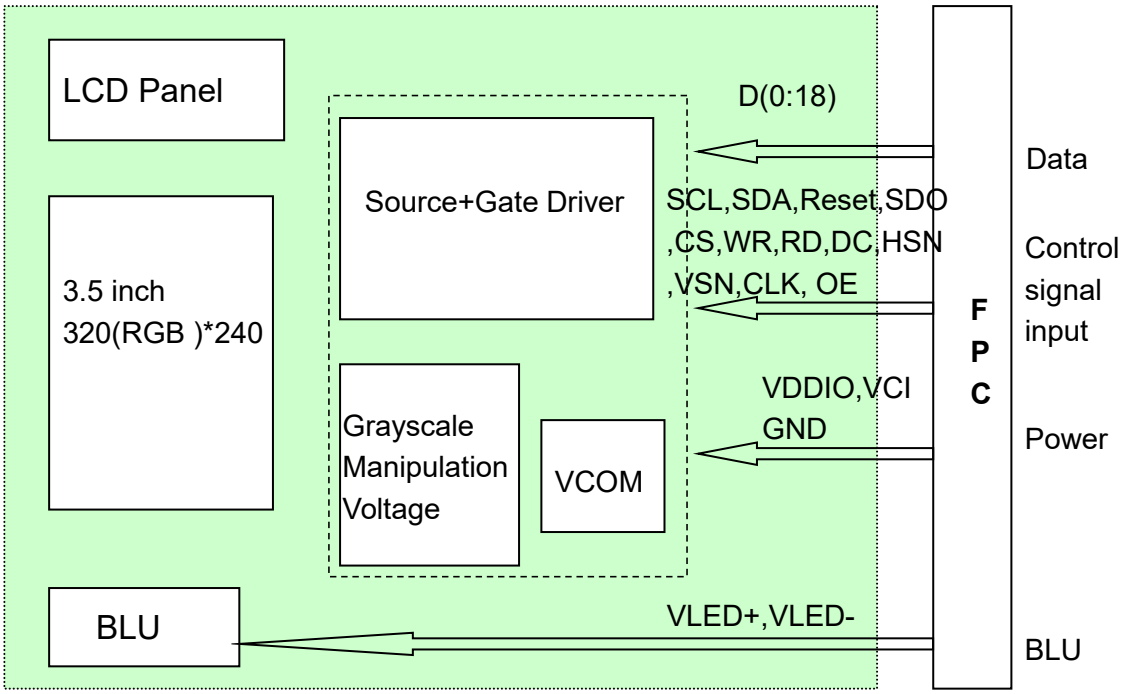
Note 1: Each LED: IF =20 mA, VF =3.2+/0.2V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

Figure: LED connection of backlight(Constant Current)

5.3 DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.6	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM}$+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA

5.4 Block Diagram



6. Interface Timing

6.1 Command

1. LCD_Initial_SSD2119:(for 16bit 8080 interface)

COMMAND	CODE	DESCRIPTION
R00H	0001	OSCEN=1
R10H	0000	Sleep=0
R07H	0033	Display control. CM=0
R11H	6870	65K color, X, Y auto increase ,updated in horizontal direction
R02H	0600	line inversion
R03H	4A38	VGH/VGL= 5/-3
R01H	72EF	Gate lines =240
R0FH	0000	Start scan line = 0
R25H	A000	Frame frequency
R28H	0006	Enable R25, R29 register
R12H	0999	Sleep mode
R26H	3800	Analogue setting
R0BH	5308	Frequency
R0CH	0003	VCIX2
R0DH	0009	VLCD63
R0EH	2300	VCOML
R1EH	0010	VCOMH
R44H	EF00	HAS and HEA station
R45H	0000	Vertical address start station
R46H	013F	Vertical address end station
R30H	0000	Gamma B control 1
R31H	0101	Gamma B control 2
R32H	0100	Gamma B control 3
R33H	0305	Gamma B control 4
R34H	0707	Gamma B control 5
R35H	0305	Gamma B control 6
R36H	0707	Gamma B control 7
R37H	0201	Gamma B control 8
R3AH	1200	Gamma B control 9
R3BH	0900	Gamma B control 10
R22H	--	Write data to RAM

2. LCD_Initial_SSD2119:(for 18bit+3wire SPI)

COMMAND	CODE	DESCRIPTION
R00H	0001	OSCEN=1
R10H	0000	Sleep=0
R07H	0033	Display control. CM=0
R11H	4E70	DFM[1:0] : 262k Color Mode DenMode = 1 : RGB interface ignore HSYNC, VSYNC pin and HBP, VBP WMode = 1 : Write RAM from Generic RGB data (POR, if PS:00xx)
R02H	0600	line inversion
R03H	6A38	VGH/VGL= 5/-3
R01H	72EF	Gate lines =240
R28H	0006	Enable R25, R29 register
R12H	0999	Sleep mode
R26H	3800	Analogue setting
R0CH	0005	VCIX2
R0DH	000D	VLCD63
R0EH	2300	VCOML
R1EH	0010	VCOMH
R15H	0058	Entry mode
R30H	0000	Gamma B control 1
R31H	0101	Gamma B control 2
R32H	0100	Gamma B control 3
R33H	0305	Gamma B control 4
R34H	0707	Gamma B control 5
R35H	0305	Gamma B control 6
R36H	0707	Gamma B control 7
R37H	0201	Gamma B control 8
R3AH	1200	Gamma B control 9
R3BH	0900	Gamma B control 10
R22H	--	Write data to RAM

6.2 AC Electrical Characteristics

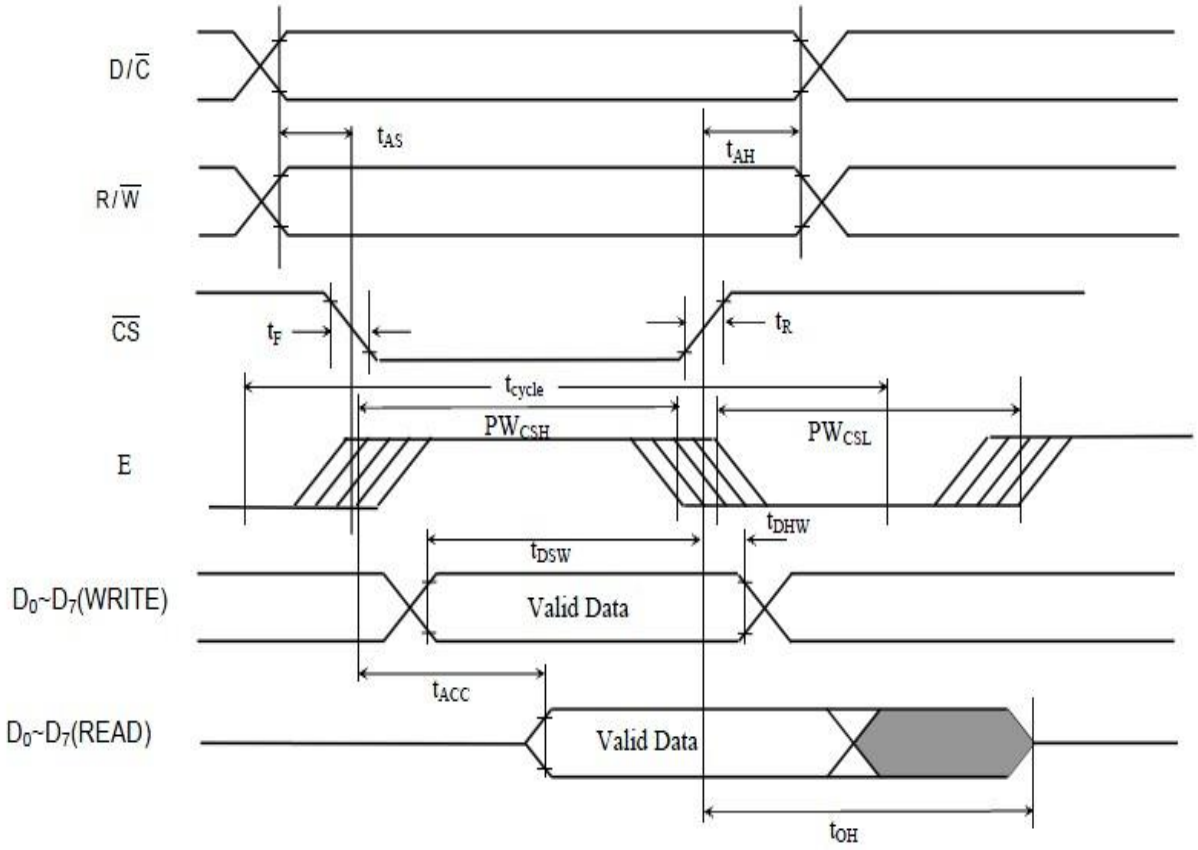
6.2.1 Parallel 6800-series Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address Setup Time (R/$\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time (R/$\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 13-1: Parallel 6800-series Interface Timing Characteristics



6.2.2 Parallel 8080 Timing Characteristics

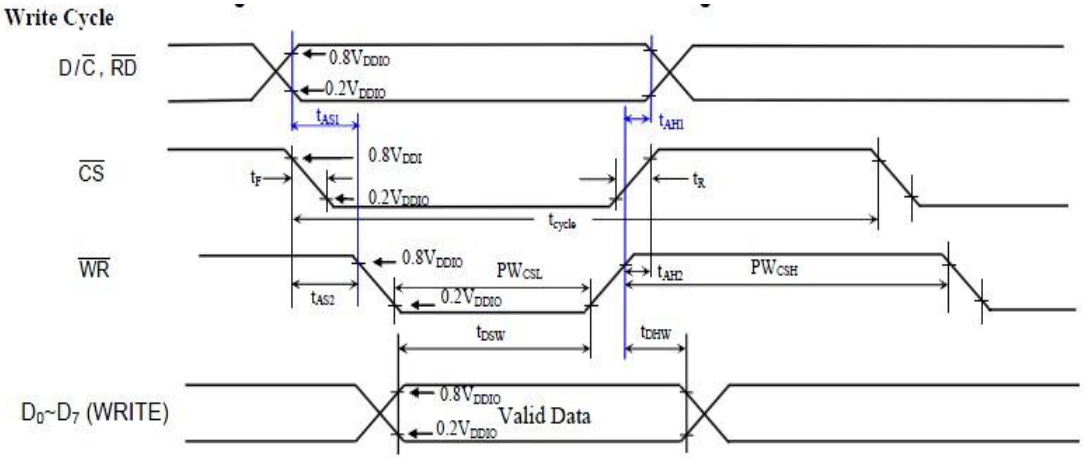
Table 13-2: Parallel 8080 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS1}	Address Setup Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

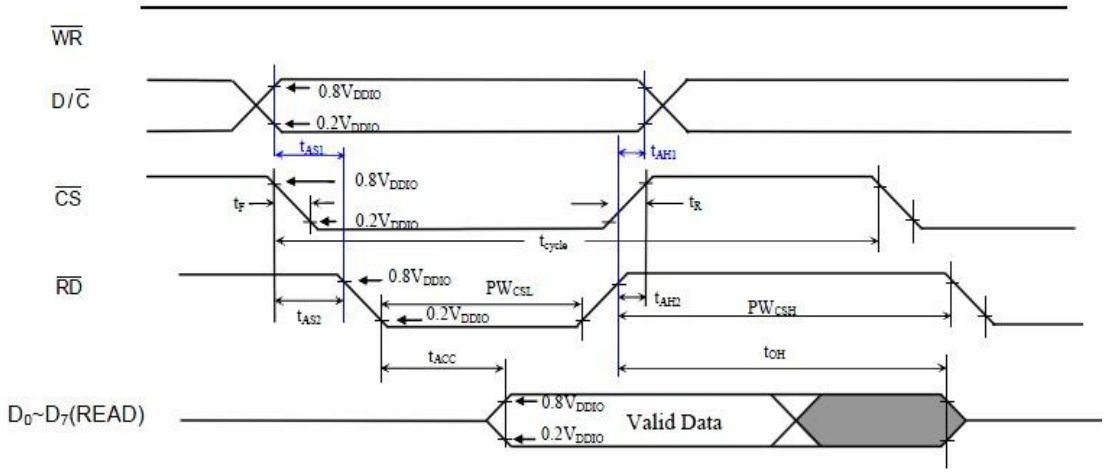
Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle



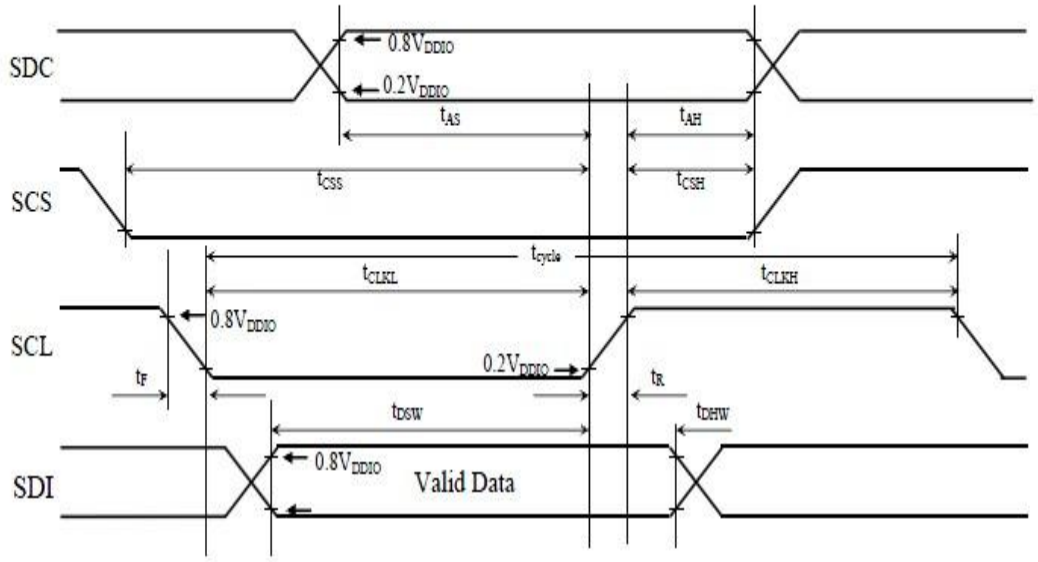
6.2.3 Serial Timing Characteristics

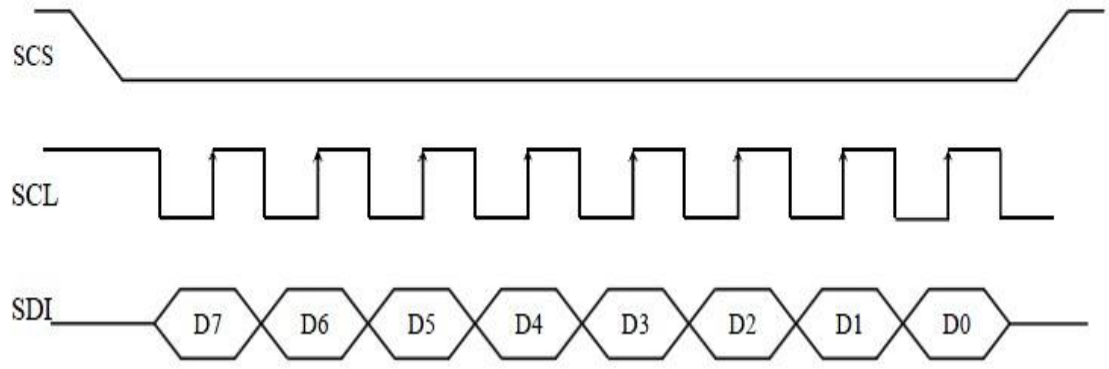
Table 13-3: Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Figure 13-3: 4 wire Serial Timing Characteristics





6.2.4 RGB Timing Characteristics

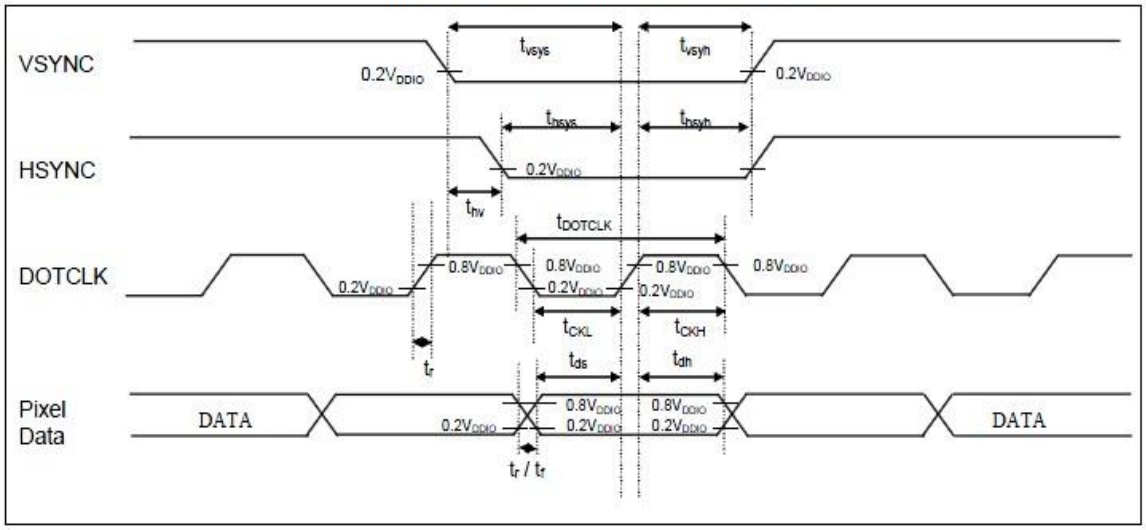
Table 13-4: RGB Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns

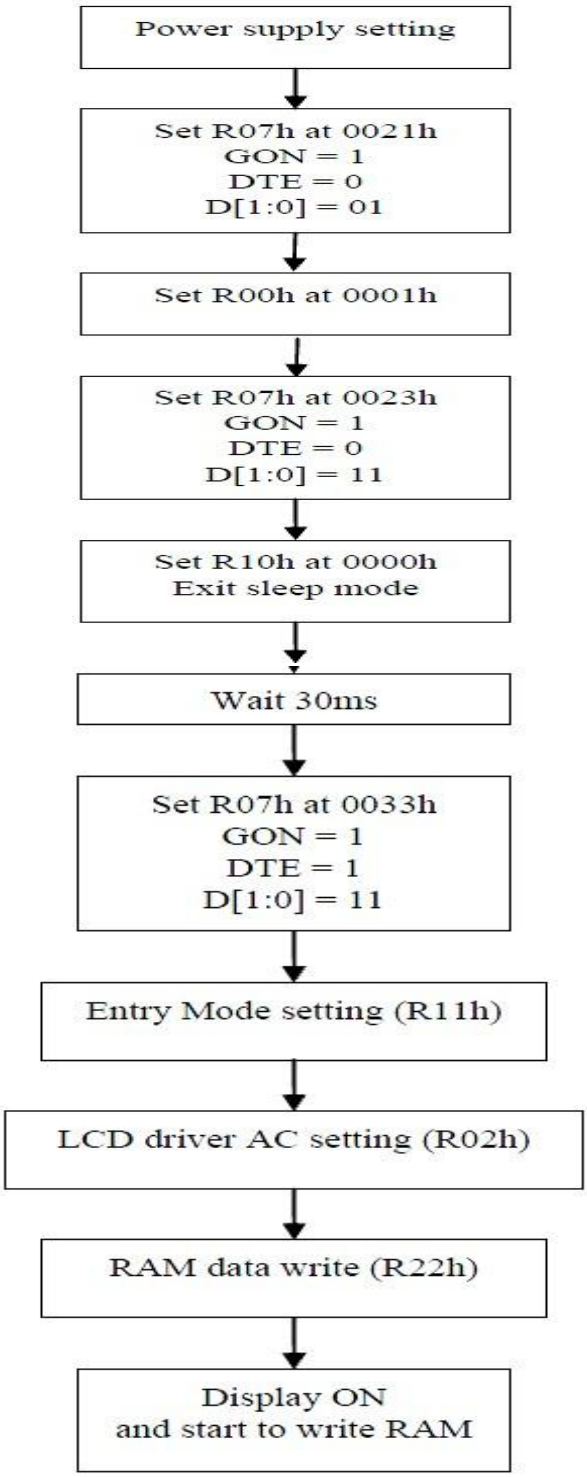
Note: External clock source must be provided to DOTCLK pin of SSD2119. The driver will not operate in absence of the clocking signal.

Figure 13-4: RGB Timing Characteristics

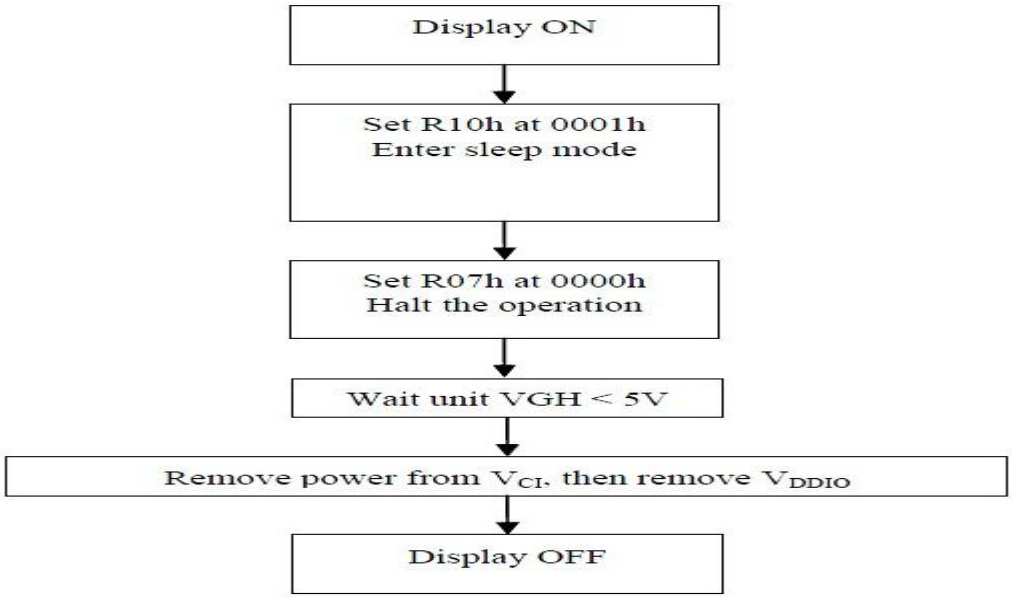


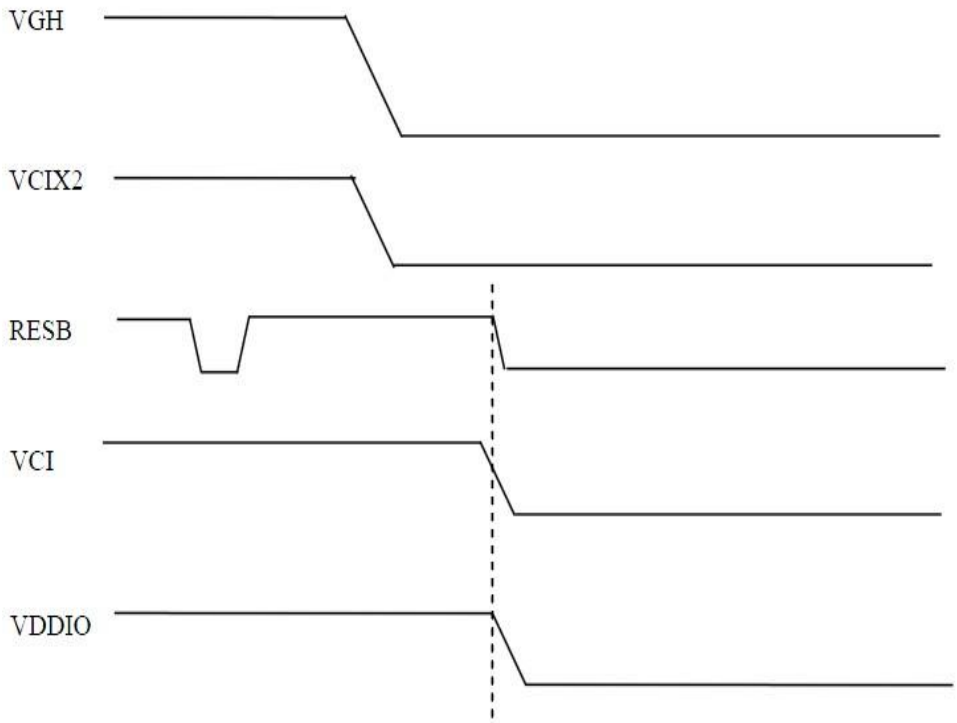
6.3 Power on/off sequence

6.3.1 Power on sequence:



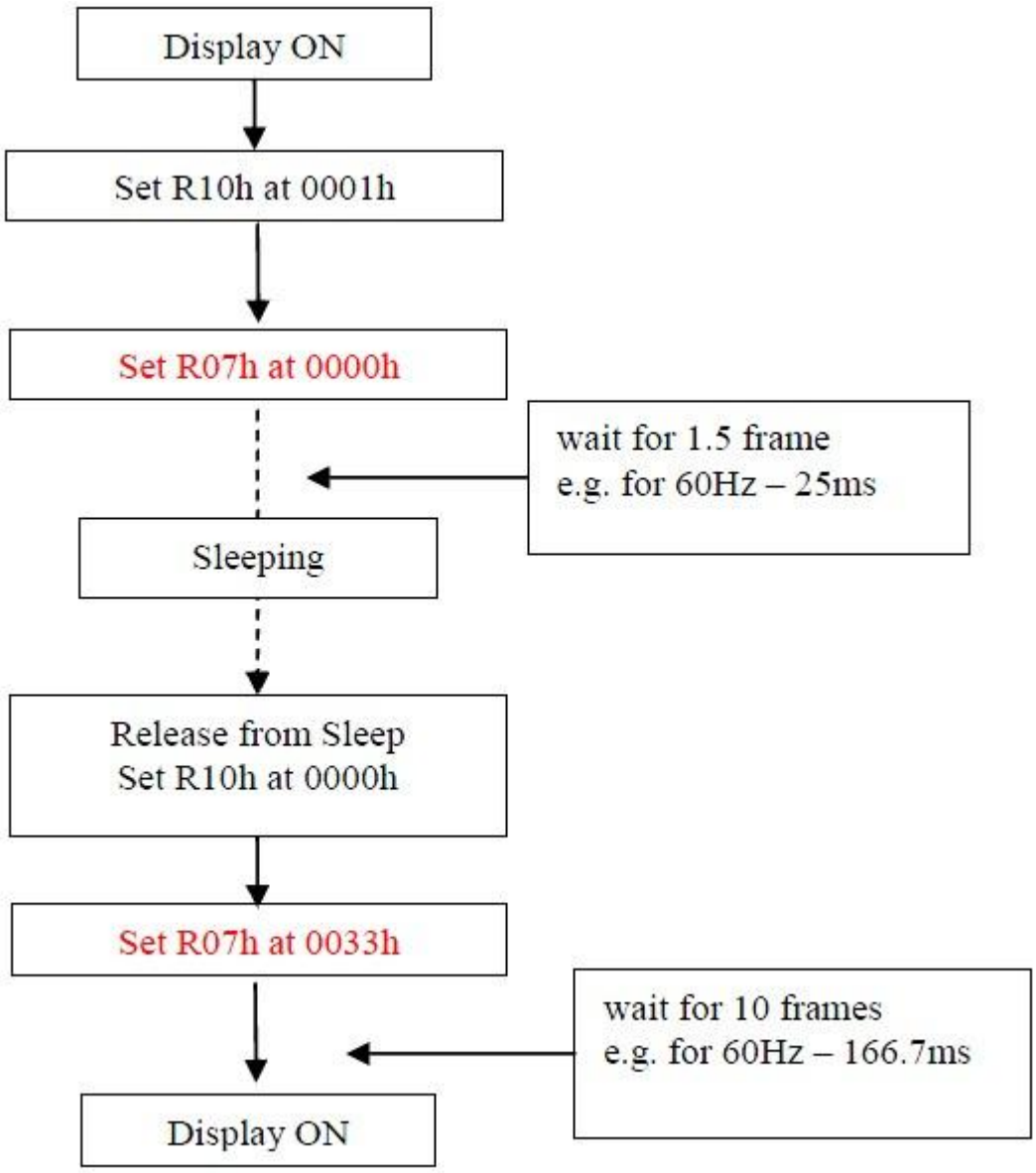
6.3.2 Display off sequence:



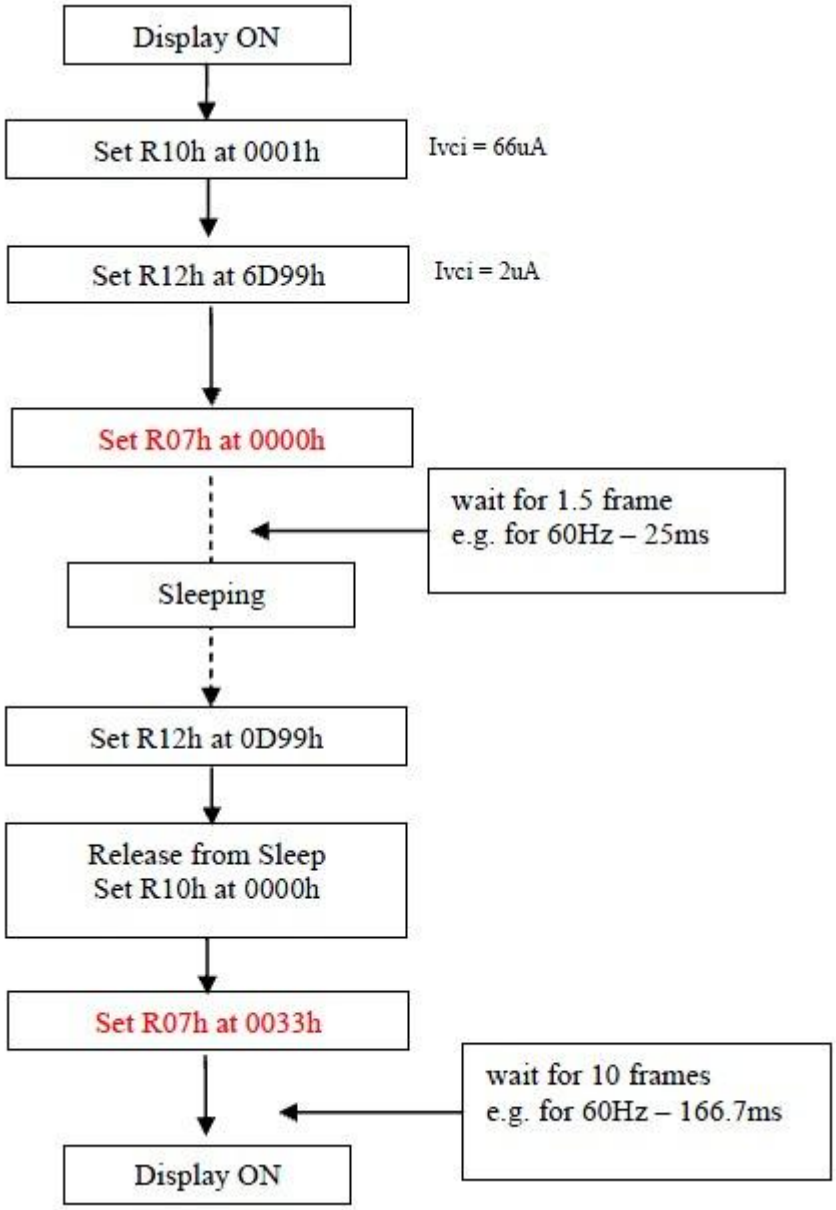


Note:
1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and cap discharged before VCI/VDDIO are turned off.

6.3.3 Sleep mode display sequence:



6.3.4 Deep sleep mode display sequence:



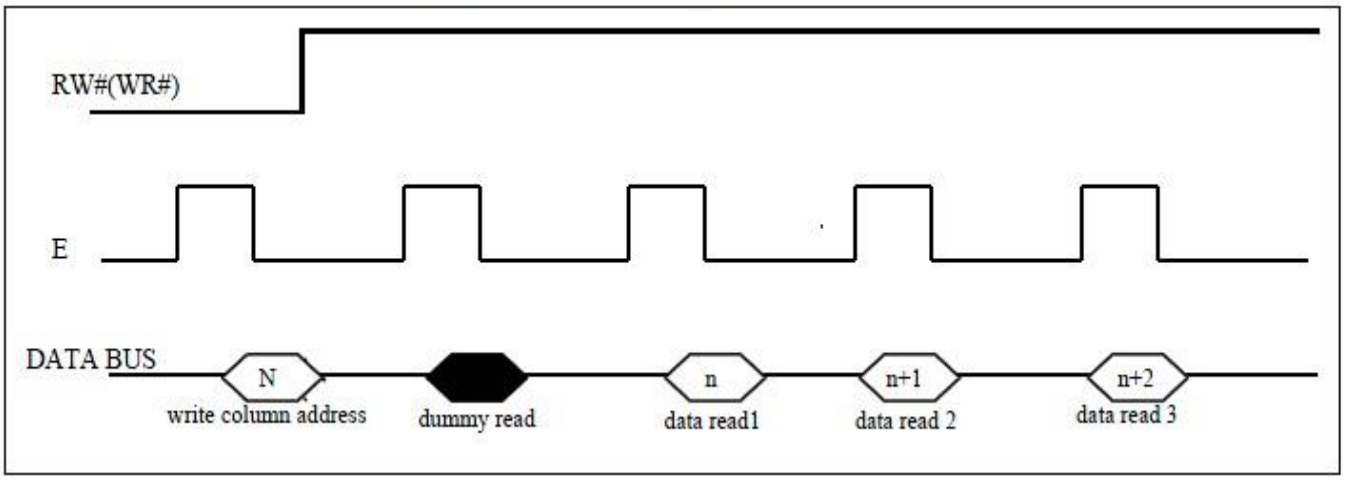
6.4 interface

6.4.1 system interface

MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins D[17:0], RW, DC, E and CS.
RW input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or status register. RW input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of DC input.
The E input served as data latch signal (clock) when high provided that CS is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

Figure 7-1: Read Display Data



MPU Parallel 8080-series Interface

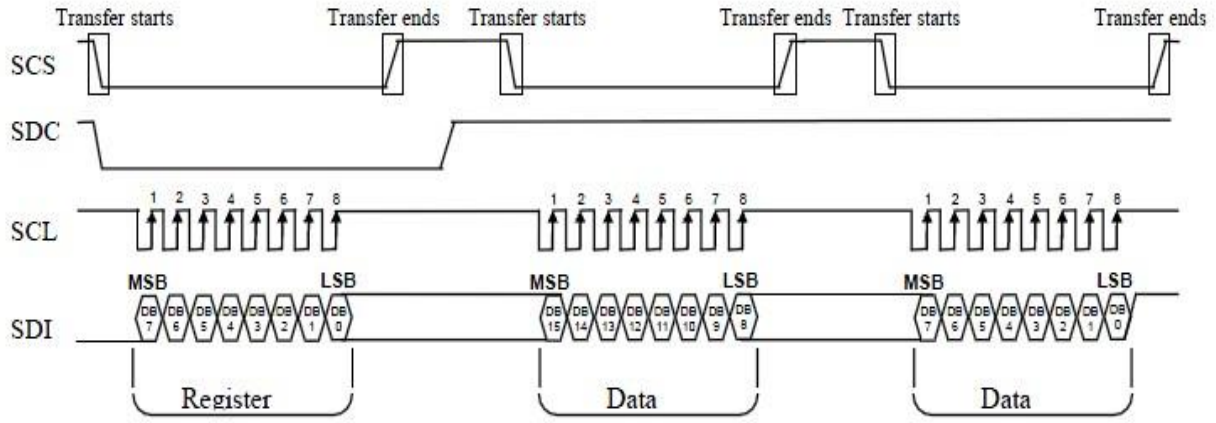
The parallel interface consists of 18 bi-directional data pins D[17:0], WR, DC, and CS.
RD input served as data read latch signal (clock) when low provided that CS is low. Weather reading the display data from GDDRAM or reading the status from the status register is controlled by DC.
WR input served as data write latch signal (clock) when low provided that CS is low. Weather writing the display data to the GDDRAM or writing the command to the command register is controlled by DC. A dummy read is also required before the first actual display data read for 8080-series interface.
Please refer to .

6.4.2 serial interface

7.1.3 4-wire Serial Peripheral Interface (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (SCS), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of SCS input and ends at the rising edge of SCS.
SDC determinates the data of SDI which is register or data.

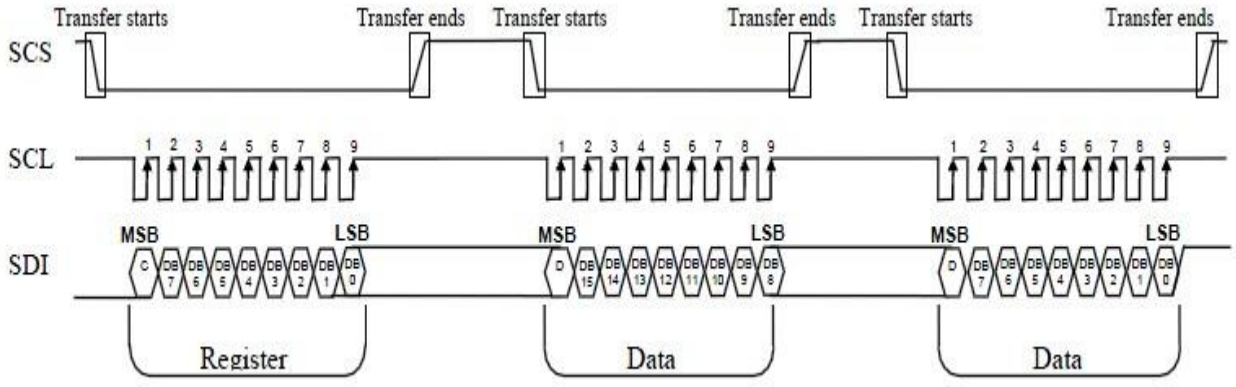
Figure 7-2: 4-wire SPI interface (8 bits)



7.1.4 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while SDC is not use. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).

Figure 7-3: 3-wire SPI interface (9 bits)



6.4.3 RGB interface

RGB Interface

SSD2119 supports RGB interface. RGB interface unit consists of D[17:0], HSYNC, VSYNC, DOTCLK and DEN signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). Data is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

6.5 command list

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R26h	Analogue Setting	0	1	0	RW_T	VCB	RLTM	ENN	0	0	0	0	0	0	0	0	0	0	0
	(3800h)			0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7. Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	50	-	ms	FIG.1	Note4
Contrast Ratio		CR		320	400	-	-	FIG.2	Note1
Surface luminance		LV	θ =0°	250	350	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	θ =0°	75	80	-	%	FIG.2	Note3
NTSC		-	θ =0°	-	50	-	%	FIG.2	Note5
Viewing angle		θ Cr>10	θ_T	-	65	-	deg	FIG.3	Note6
			θ_B	-	55	-	deg	FIG.3	
			θ_L	-	65	-	deg	FIG.3	
			θ_R	-	65	-	deg	FIG.3	
Chromaticity	Red	R_X	θ =0° ∅ =0° Ta=25°	0.585	0.635	0.685	-	FIG.2 CIE1931	Note5
		R_Y		0.299	0.349	0.399	-		
	Green	G_X		0.099	0.149	0.199	-		
		G_Y		0.032	0.082	0.132	-		
	Blue	B_X		0.338	0.388	0.438	-		
		B_Y		0.545	0.595	0.645	-		
	White	W_X		0.279	0.329	0.379	-		
		W_Y		0.284	0.334	0.384	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and

"Black"state.Rise time (Tr) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Tf) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers' s ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

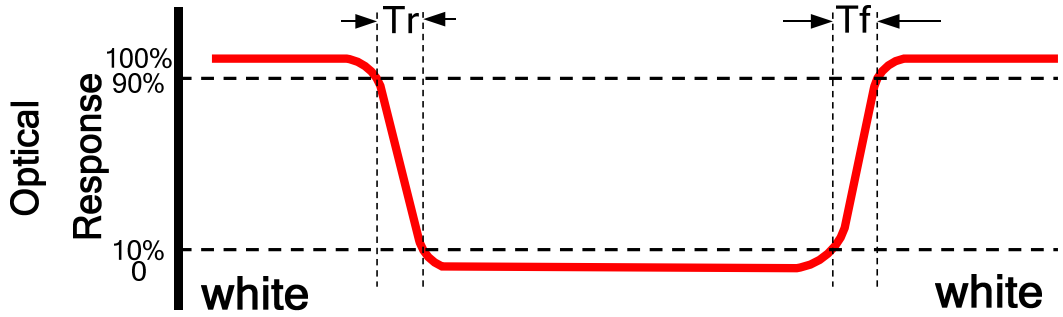


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

Size : S≤5"(see Figure a) A : 5 mm B : 5 mm
H,V : Active area

Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

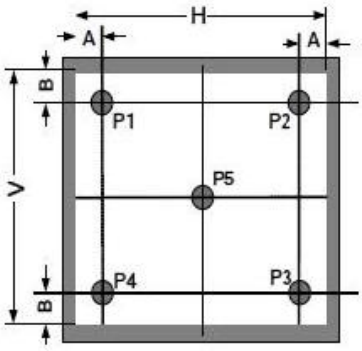


Figure a

Size : 5”＜S≤12.3”(see Figure b) H,V : Active area

Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON’s luminance meter BM-5 or BM-7 or compatible (see Figure c).

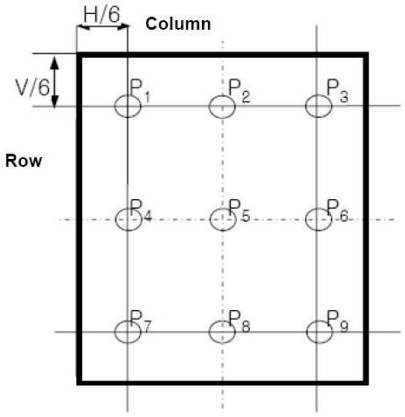


Figure b

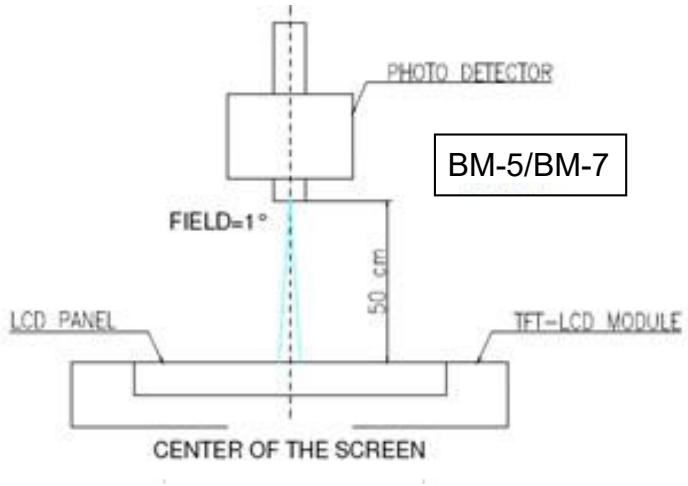
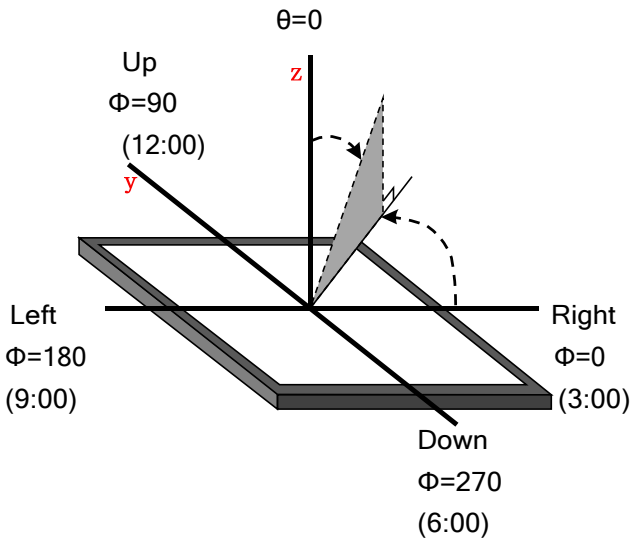


Figure c

FIG.3.The definition of viewing angle

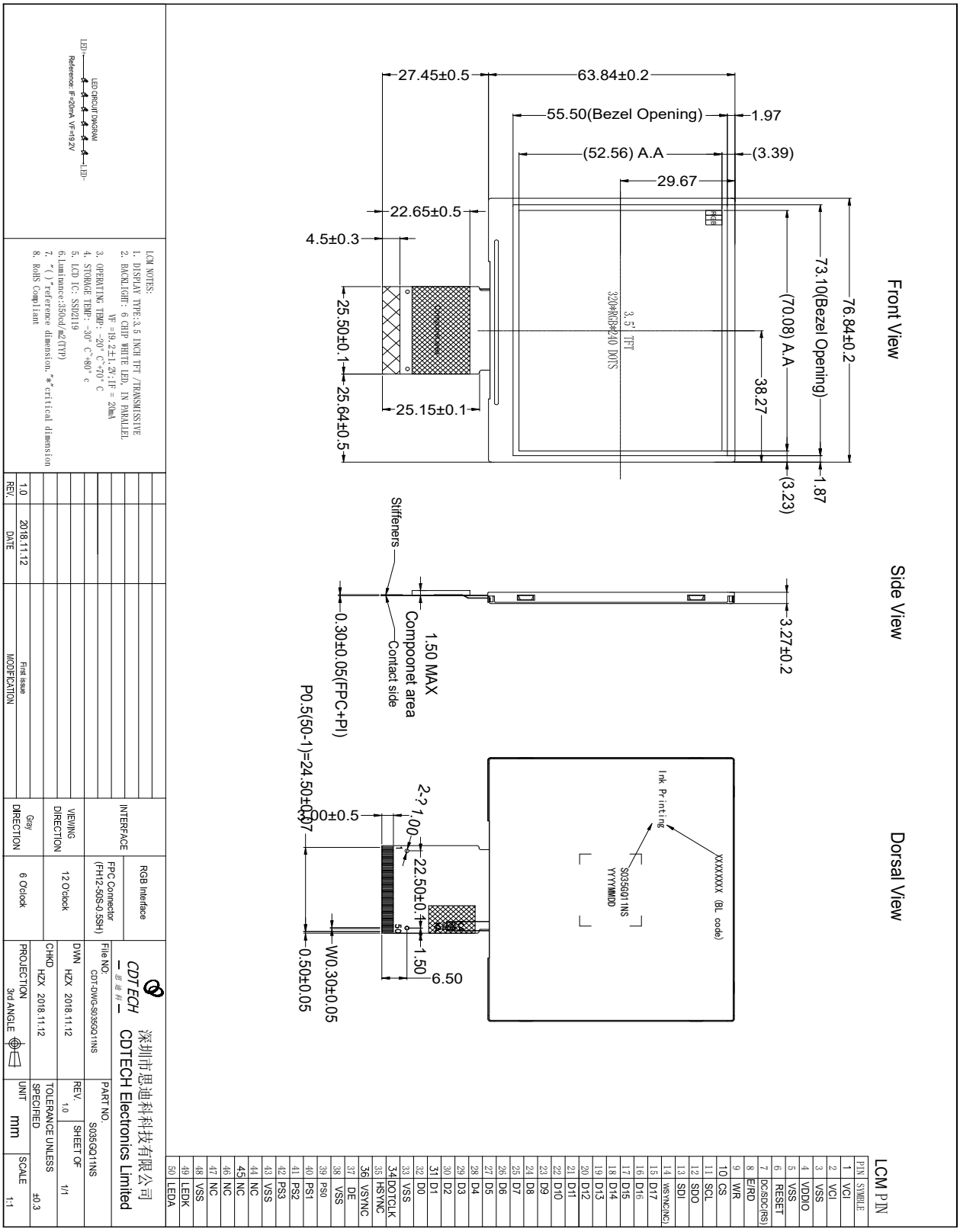


8. Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 120hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 120hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max,120 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20℃ 30 min ~ +60℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note:1. Ts is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.
3. The size of sample is 5pcs.

9. Mechanical Drawing



10. Packing

Packing Method

TBD

11. Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.