

PRODUCT SPECIFICATION

CDTECH Model: **S101QWU65HP**

CUSTOMER Model: **-**

Description: **10.1" TFT-LCD Module**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
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Record of Revisions

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Contents

1. General Specifications	4
2. Absolute Maximum Ratings	4
3. Electrical Characteristics	5
4. Interface Pin Assignment	6
5. Interface Characteristics	7
6. Optical Specifications	11
7. Reliability Test Items	14
8. Mechanical Drawing	15
9. Packing	16
10. Precautions for Use of LCD modules	17

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	10.1	inch
Number of Pixels	1200 (H) RGB x 1920 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	o' clock
Interface	MIPI	-
Display Colors	16.7M	colors
Outline Dimension	142.50 (H) x 227.93 (V) x 3.00 (D)	mm
Active Area	135.36 (H) x 216.58 (V)	mm
Pixel Pitch	0.1128 (H) x 0.1128 (V)	mm
Driver IC	HX8279	-
Operation Temperature	-10~60	°C
Storage Temperature	-20~70	°C

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	5.0	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.

Functional operation should be restricted to the conditions described under normal operating conditions.

3. Electrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

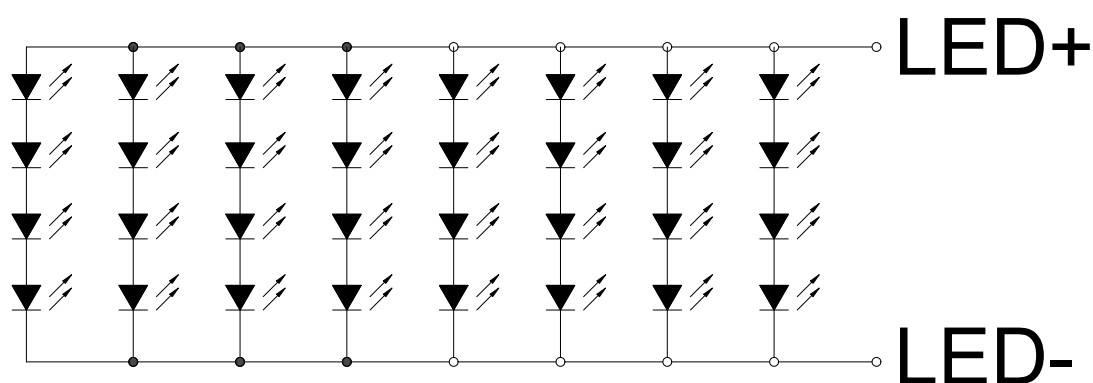
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VCC	3.0	3.3	3.6	V	
Analog supply current	I _{VCC}	-	TBD	-	mA	VCC=3.3V
Logic input voltage	VIH	0.7*VCC	-	VCC	V	
	VIL	GND	-	0.3*VCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I _F	-	160	-	mA	
Driving Voltage	V _F	22.4	-	25.6	V	
Power consumption	W _{BL}	3.584	-	4.096	W	
LED Life-Time	N/A	30,000	-	-	Hours	Ta=25°C Note 1

Note 1: LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2: LED circuit :



4. Interface Pin Assignment

4.1 LCM Pin Assignment

Recommended connector: FH12-40S-0.5SH manufactured by HIROSE

No.	Symbol	Description
1	NC	No connection
2	VCC_LCD3.3V	Power supply (3.3V)
3	VCC_LCD3.3V	Power supply (3.3V)
4	NC	No connection
5	RESET	Global reset pin
6	NC	No connection
7	GND	Ground
8	MIPI_D2N	MIPI Negative data signal(-)
9	MIPI_D2P	MIPI Positive data signal(+)
10	GND	Ground
11	MIPI_D1N	MIPI Negative data signal(-)
12	MIPI_D1P	MIPI Positive data signal(+)
13	GND	Ground
14	MIPI_CKN	MIPI Negative clock signal(-)
15	MIPI_CKP	MIPI Positive clock signal(+)
16	GND	Ground
17	MIPI_D0N	MIPI Negative data signal(-)
18	MIPI_D0P	MIPI Positive data signal(+)
19	GND	Ground
20	MIPI_D3N	MIPI Negative data signal(-)
21	MIPI_D3P	MIPI Positive data signal(+)
22	GND	Ground
23	NC	No connection
24	NC	No connection
25	GND	Ground
26	NC	No connection
27	NC	No connection
28	NC	No connection
29	NC	No connection
30	GND	Ground
31	VLED-	Power for LED backlight (Cathode)
32	VLED-	Power for LED backlight (Cathode)
33-38	NC	No connection
39	VLED+	Power for LED backlight (Anode)
40	VLED+	Power for LED backlight (Anode)

5. Interface Characteristics

5.1 Reset Timing Characteristics

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, T_{OPR} = -20℃~+85℃)

Parameter	Symbol	Conditions	Min.	Spec. Typ.	Max.	Unit
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.5: Reset timing

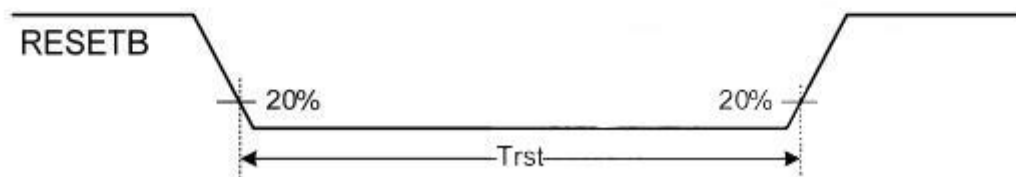


Figure 13.6: Reset timing

The diagram illustrates the timing requirements for the HS-LVDS interface, divided into two main sections: Clock Lane and Data Lane.

Clock Lane Dp/Dn: This section shows the clock signal transitions. Key timing parameters include:

- T_{CLK_POST} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{CLK_MISS} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{EQT} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{CLK_SETTLE} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- $T_{CLK_TERM_EN}$: Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{CLK_TRAIL} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{HS_EXIT} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{LPX} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- $T_{CLK_PREPARE}$: Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{CLK_ZERO} : Time from the start of the clock signal to the point where the signal is no longer sampled.
- T_{CLK_PISE} : Time from the start of the clock signal to the point where the signal is no longer sampled.

Data Lane Dp/Dn: This section shows the data signal transitions. Key timing parameters include:

- T_{HS_SKIP} : Time from the start of the data signal to the point where the signal is no longer sampled.
- T_{LPX} : Time from the start of the data signal to the point where the signal is no longer sampled.
- $T_{HS_PREPARE}$: Time from the start of the data signal to the point where the signal is no longer sampled.
- $T_{D_TERM_EN}$: Time from the start of the data signal to the point where the signal is no longer sampled.
- T_{HS_SETTLE} : Time from the start of the data signal to the point where the signal is no longer sampled.

The diagram also indicates the presence of a "Disconnect Terminator" at the end of the signal lines.

Timing diagram for the first data bit capture in a Dp/Dn lane. The diagram shows the relationship between the Clock Lane (Dp/Dn) and the Data Lane (Dp/Dn). Key timing parameters include T_{LPX} , $T_{HS_PREPARE}$, T_{HS_ZERO} , T_{HS_SYNC} , $T_{TERMENH}$, T_{TERM} , $T_{TERMOUT}$, $T_{TERMSTR}$, and $T_{TERMEXIT}$. The diagram also shows the signal levels $-V_{IH(min)}$, $-V_{IL(max)}$, and $-V_{TERMENH(max)}$. The first data bit is captured during the $T_{TERMENH}$ period. The diagram is divided into LP-11, LP-01, and LP-00 phases.

The diagram illustrates the timing sequence for the LPX pin. It shows two transitions: a high-to-low transition (left) and a low-to-high transition (right). The states of the pin are labeled as LP-11, LP-10, LP-00, LP-10, and LP-11. Key timing parameters are indicated by arrows above the transitions: T_{LPX} (LPX pulse width), T_{TA-GO} (time from LP-00 to TA-GET), and $T_{TA-SURE}$ (time from LP-00 to TA-SURE). A 'drive overlap' period is shown where both TA-GET and TA-SURE are active. The low-to-high transition is also labeled with T_{LPX} and T_{TA-GET} .

MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T _{REOT}	30%-85% rise time and fall time	-	-	35	ns
T _{CLK-MISS}	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
T _{CLK-POST} *1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T _{HS-TRAIL} to the beginning of T _{CLK-TRAIL} .	60 ns + 52*UI (For DCS)	-	-	ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
T _{CLK-SETTLE}	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of T _{CLK-PRE} .	95	-	300	ns
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V _{IL,MAX} .	Time for Dn to reach V _{TERM-EN}	-	38	ns
T _{HS-SETTLE}	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of T _{HS-PREPARE} .	85 ns + 6*UI	-	145 ns + 10*UI	ns
T _{EOT}	Time from start of T _{HS-TRAIL} or T _{CLK-TRAIL} period to start of LP-11 state	-	-	105ns+48*UI	-
T _{HS-EXIT} ⁽¹⁾	time to drive LP-11 after HS burst	100	-	-	ns
T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
T _{HS-PREPARE} + T _{HS-ZERO}	T _{HS-PREPARE} + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
T _{HS-SKIP}	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T _{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T _{LPX}	Ratio of T _{LPX(MASTER)} /T _{LPX(SLAVE)} between Master and Slave side	2/3	-	3/2	-
T _{TA-GET}	Time to drive LP-00 by new TX	5*T _{LPX}			ns
T _{TA-GO}	Time to drive LP-00 after Turnaround Request	4*T _{LPX}			ns
T _{TA-SURE}	Time-out before new TX side starts driving	T _{LPX}	-	2*T _{LPX}	ns

Note: (1) For image transmission:

T_{CLK-POST} min value = 164 when MIPI max frequency per lane = 0.53Gbps.

T_{CLK-POST} min value = 112 when MIPI max frequency per lane = 1Gbps

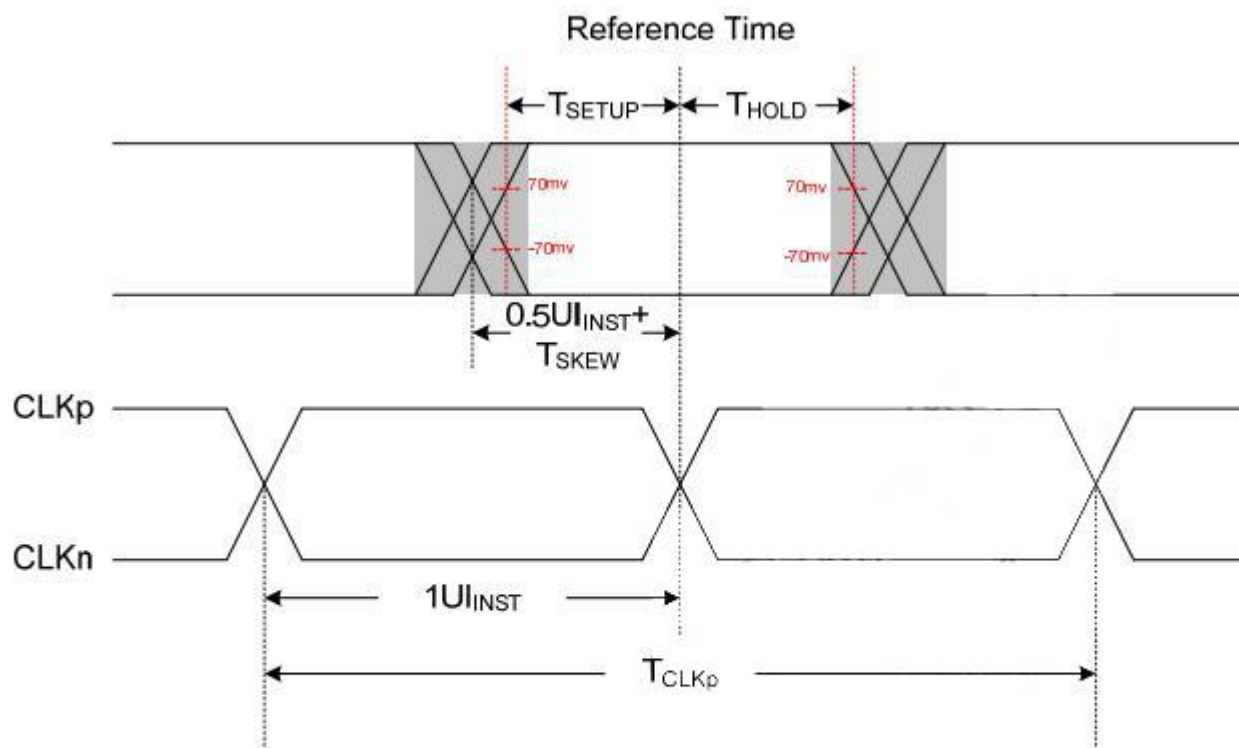


Figure 13.4: Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	U_{INST}	1.0	-	12.5 ⁽¹⁾	ns
Data to clock setup time	T_{SETUP}	0.15	-	-	U_{INST}
Data to clock hold time	T_{HOLD}	0.15	-	-	U_{INST}

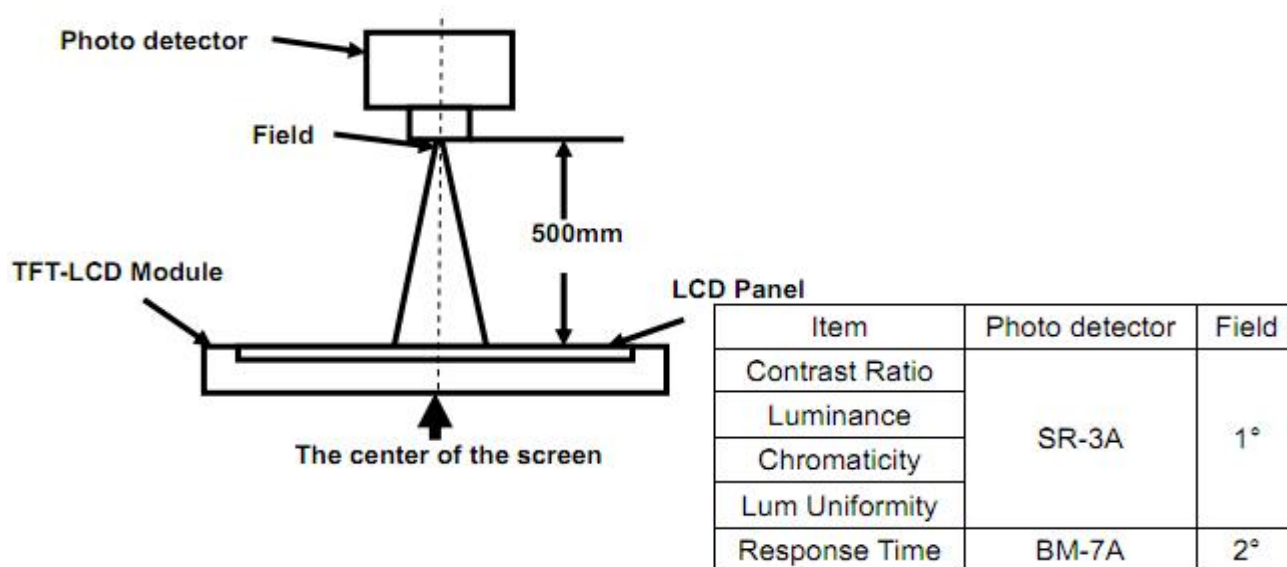
Note: (1) This value corresponds to a minimum 80 Mbps data rate.

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	$\Phi=90^\circ$ (12 o'clock)	80	85	-	deg	Note2
	θ_B	$\Phi=270^\circ$ (6 o'clock)	80	85	-	deg	Note2
	θ_L	$\Phi=180^\circ$ (9 o'clock)	80	85	-	deg	Note2
	θ_R	$\Phi=0^\circ$ (3 o'clock)	80	85	-	deg	Note2
Response Time	T_{ON}	Normal $\theta=\Phi=0^\circ$	-	12	-	msec	Note4
	T_{OFF}		-	12	-	msec	Note4
Contrast Ratio	CR		800	1000	-	-	Note1 Note3
Color Chromaticity	W_X		0.280	0.300	0.320	-	Note1 Note5
	W_Y		0.305	0.325	0.345	-	Note1 Note5
Luminance	L		500	600	-	cd/m ²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		-	65	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system

Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

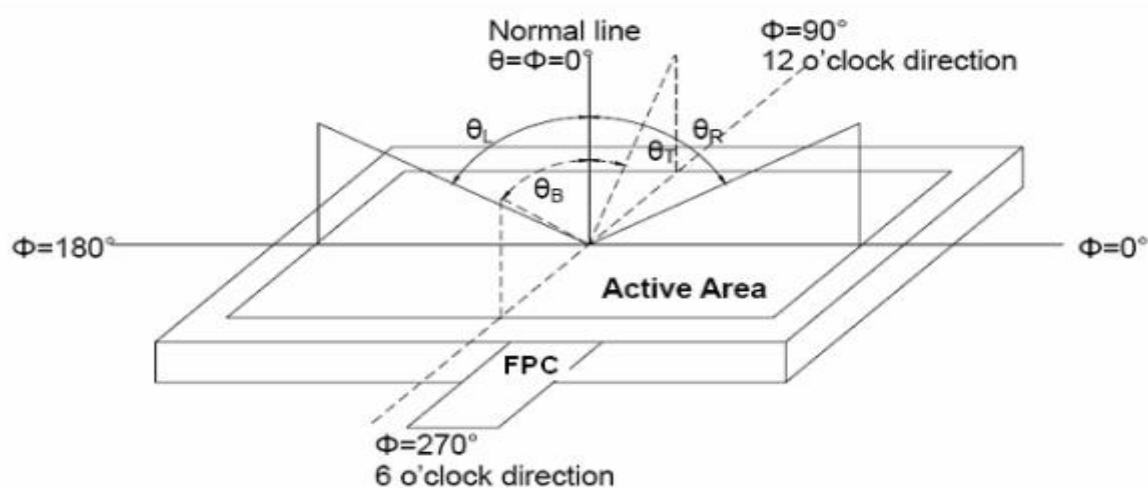


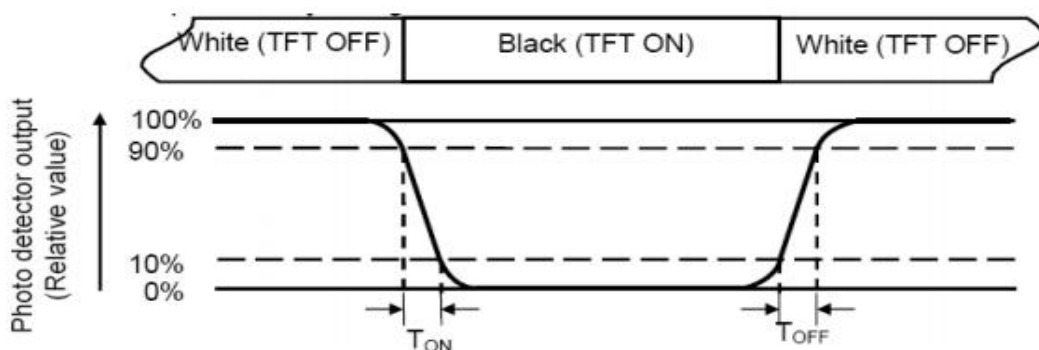
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

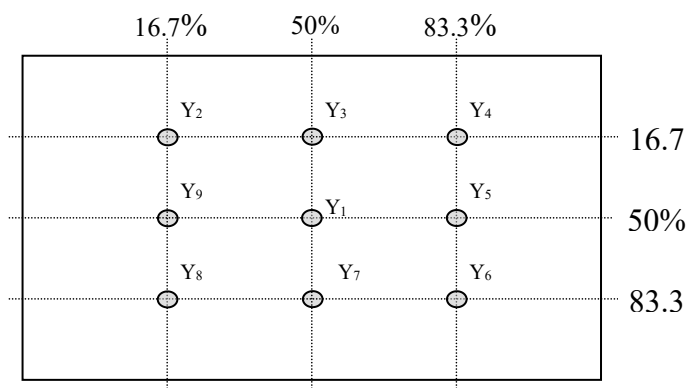


Fig. 2 Definition of points

Note 7: Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

L_v = Average Surface Luminance with all white pixels($P_1, P_2, P_3, \dots, P_n$).

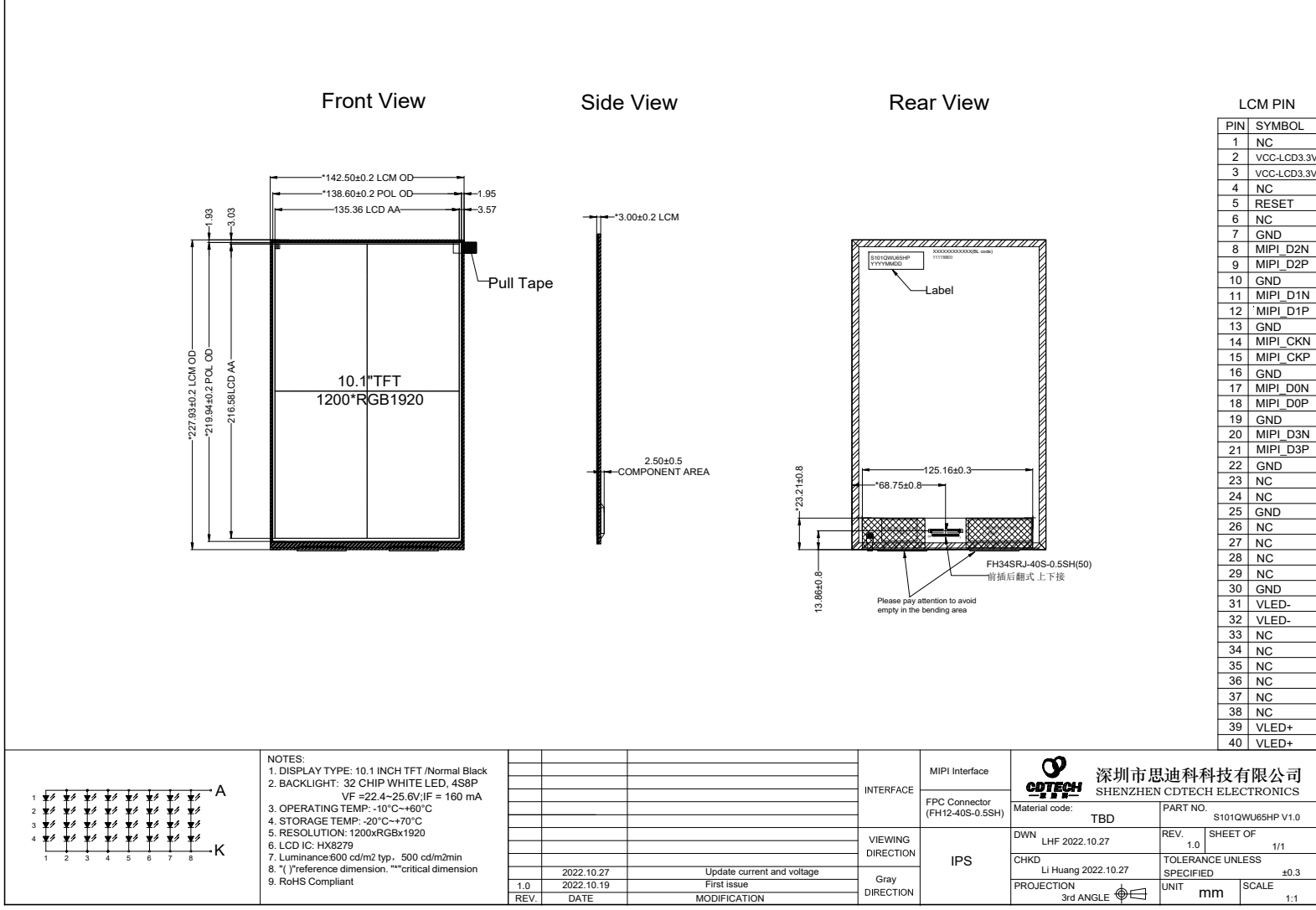
7. Reliability Test Items

Test Item	Test Conditions
High Temperature Storage	Ta= +70℃ 96hrs
Low Temperature Storage	Ta= -20℃ 96hrs
High Temperature Operation	Ta= +60℃ 96hrs
Low Temperature Operation	Ta= -10℃ 96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH 96hrs
Thermal Shock (Non-operation)	-20℃/30 min ~ +70℃/30 min for 20 cycles Start with cold temperature end with high temperature
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

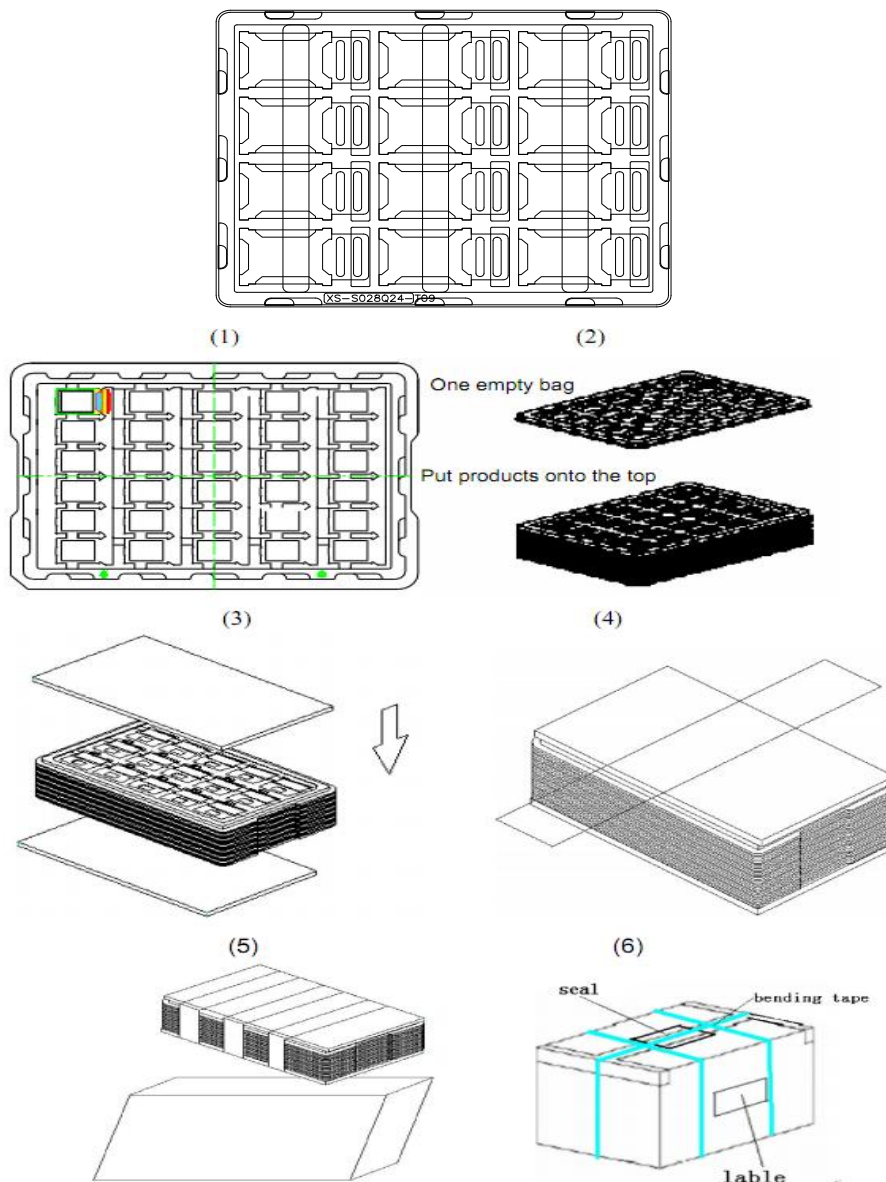
- 1). Air bubble in the LCD
- 2). Seal leak or Glass crack
- 3). Non display or abnormal display
- 4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2. The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time, the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.