

Product Specification

Model Name	S050BWQ65HG
Description	Standard LCD Module 5.0" WQVGA 480(RGB)x272 Dots
Date	2018/11/22
Version	1.0

Approved by/Date	Check by/Date	Prepared by/Date
	ZHP 2018/11/22	Yigui.Han 2018/11/22

Customer Approval	
Date	



CDTech(H.K.)Electronics Limited

Table of Contents

1. Record of Revision	3
2. General Specifications	4
3. Input/OutputTerminals	5
4. Absolute Maximum Rating	6
5. Electrical Characteristics.....	6
6. Interface Timing.....	8
7. Optical Characteristics	15
8. Environmental / Reliability Tests	19
9. Mechanical Drawing	20
10. Packing	21
11. Precautions for Use of LCD modules	22

1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2018/11/22	First Release.	Yigui.Han

2. General Specifications

Feature		Spec
Characteristics	Size	5 inch
	Resolution	480(horizontal)*272(Vertical)
	Interface	RGB-24bit
	Connect type	Connector
	Display Colors	16.7M
	Technology type	a-Si
	Pixel pitch (mm)	0.231*0.231
	Pixel Configuration	R.G.B.-Stripe
	Display Mode	Normally White
	LCD Driver IC	HX8257A-M
	Viewing Direction	12 O'clock
	Gray Inversion Direction	6 O'clock
Mechanical	LCM (W x H x D) (mm)	120.70*75.80*2.8
	Active Area(mm)	110.88 x62.83
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	12 LEDs

Note 1: Requirements on Environmental Protection: RoHs

Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

No.	Symbol	Description
1	VLED-	Backlight LED Cathode
2	VLED+	Backlight LED Anode.
3	GND	Ground
4	VDD	Power supply
5~12	R0~R7	Data bus
13~20	G0~G7	Data bus
21~28	B0~B7	Data bus
29	GND	Ground
30	DCLK	Dot clock signal input. Latching input data at its rising edge.
31	DISP	Standby mode. Normally pulled high. DISP="1": Normally operation (Default) DISP="0": Timing controller, source driver will turn off ,all output are High-Z.
32	NC	No connected
33	NC	No connected
34	DE	Data enable input. Active high to enable the input data bus under "DE Mode."
35	NC	No connected
36	GND	Ground
37	XR(NC)	The right side signal of TP
38	YD(NC)	The down side signal of TP
39	XL(NC)	The left side signal of TP
40	YU(NC)	The up side signal of TP

4. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	-	5	V	-
Operating Temperature	TOPR	-20	-	70	°C	-
Storage Temperature	TSTG	-30	-	80	°C	-

5. Electrical Characteristics

5.1 Driving TFT LCD Panel

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input Signal Voltage	Low Level	V _{IL}	GND	-	0.3x VDD	V
	High Level	V _{IH}	0.7x VDD	-	VDD	V
Output Signal Voltage	Low Level	V _{IL}	-	-	VSS+0.4	V
	High Level	V _{IH}	VDD-0.4	-	-	V
(Panel+LSI) Power Consumption	Black Mode (60Hz)	-	-	-	nW	
	Standby	-	-	-	uW	

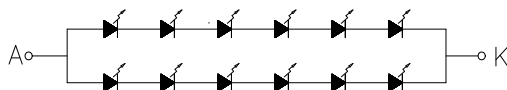
5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I _F	-	40	50	mA	
Forward Voltage	V _F	18	19.2	20.4	V	
Backlight Power consumption	W _{BL}	-	0.768	-	W	
LED Lifetime		-	30000	-	Hrs	

Note 1: Each LED: I_F =20 mA, V_F =3.2+/-0.2V.

Note 2: Optical performance should be evaluated at Ta=25°C only.

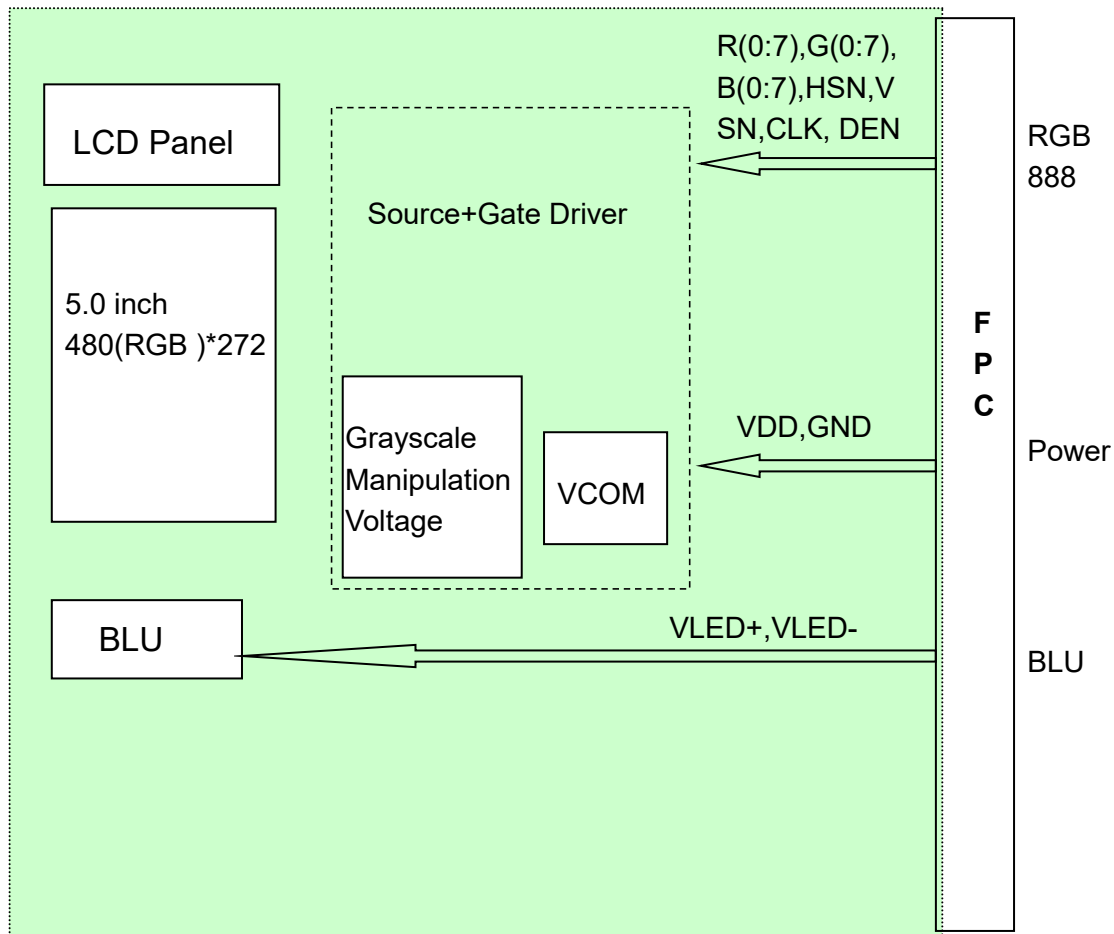
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.



CIRCUIT DIAGRAM

Figure: LED connection of backlight(Constant Current)

5.3 Block Diagram



6. Interface Timing

6.1 DC characteristics

(Unless otherwise specified, Voltage Referenced to DVSS, VDDIO = 2.2V, T_A = 25 °C)

Symbol	Parameter	Test condition	Min.	Spec. Typ.	Max.	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.8	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	$\geq$ VDDIO & ≥ 3	-	3.6	V
I _{sleep}	Sleep mode current	-	-	50		μA
I _{VCI}	VCI Operating mode current	VCI=3.3V · VDDIO=3.3V at Black Pattern with 4.3" Panel	-	13	16	mA
VCL	Negative V _{CI} Output Voltage	No panel loading	- VCI	-	- VCI+0.7	V
VCIX2	VCIX2 primary booster efficiency ⁽³⁾	No panel loading, ITO for VCIX2, VCI and VCHS = 10 Ohm	5.2	5.4	5.6	V
VDC	VDC Output Voltage	VDC[3:0]=1011	4.9	5	5.1	V
VGH	Gate driver High Output Voltage Booster efficiency ⁽¹⁾	No panel loading; 3x booster	84	89.5	-	%
		No panel loading; 4x booster	80	88.5	-	%
VGL	Gate driver Low Output Voltage	VGL= -2 x VDC VDC[3:0]=1011	-10	-10	-9	V
COMH	VCOM High Output Voltage ⁽²⁾	-	-3%	COMC+COMPP	3%	V
COML	VCOM Low Output Voltage ⁽²⁾	-	-3%	COMC-COMPP	3%	V
VLCD	VLCD Output Voltage	VRH[5:0]=110011	5.0	5.1	5.2	V
V _{OH1}	Logic High Output Voltage	I _{out} = -100μA	0.9*VDDIO	-	VDDIO	V
V _{VD}	Source Output Voltage Deviation	-	-	±20	±30	mV
V _{OS}	Source Output Voltage Offset	-	-	-	±30	mV
V _{OL1}	Logic Low Output Voltage	I _{out} = 100μA	0	-	0.1*VDDIO	V
V _{IH1}	Logic High Input voltage	2.5V < VDDIO < 3.6V 1.8V < VDDIO ≤ 2.5V	0.7*VDDIO 0.8*VDDIO	-	VDDIO	V
V _{IL1}	Logic Low Input voltage	2.5V < VDDIO < 3.6V 1.8V < VDDIO ≤ 2.5V	0	-	0.3*VDDIO 0.2*VDDIO	V
I _{OH}	Logic High Output Current Source	V _{out} = VDD - 0.4V	50	-	-	μA
I _{OL}	Logic Low Output Current Drain	V _{out} = 0.4V	-	-	-50	μA
I _{OZ}	Logic Output Tri-state Current Drain Source	-	-1	-	1	μA
I _{IL/IH}	Logic Input Current	-	-1	-	1	μA

Note : (1) VGH efficiency = VGH / (VDC x n) x 100% (where n = booster factor)

(2) COML < 0V, COMH < VCIX2J, COMH > VCI

(3) VCIX2 voltage is related with VCI voltage & VCIX2 loading. Figure10.1 shows the estimated VCIX2 voltage under different VCIX2 current loading when ITO for VCIX2 · VCI and VCHS = 10Ω.

6.2 AC characteristics

6.2.1 Timing relationship among DE,Source Output,Gate Output,VCOM

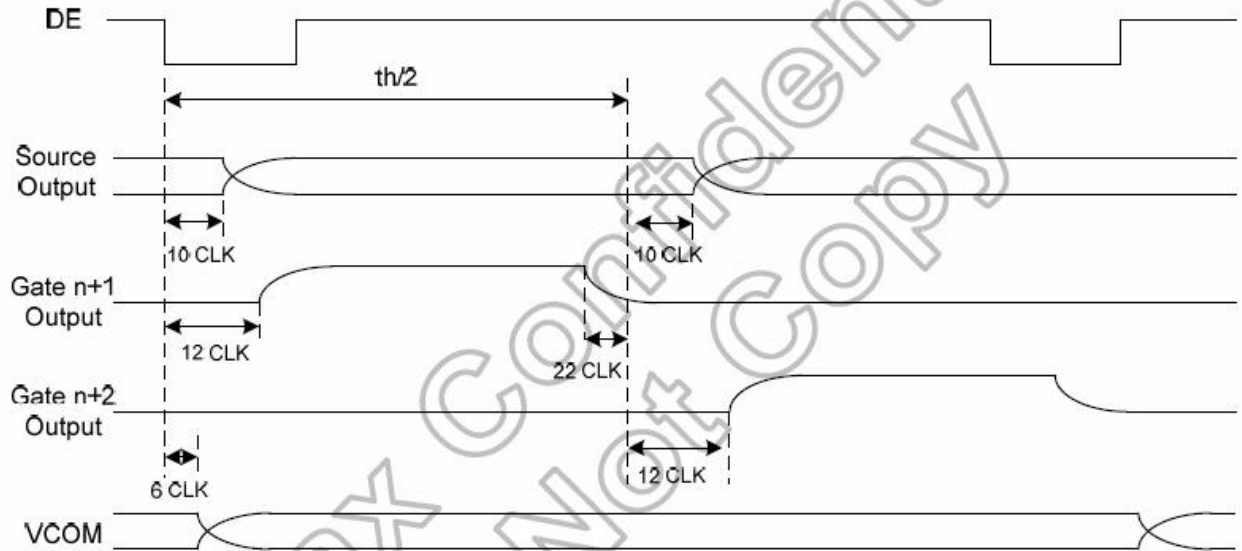


Figure 11.1 Timing Relationship

6.2.2 Parallel RGB input timing requirement

(480RGBx272, $T_A=25^{\circ}\text{C}$, VDDIO=1.8V to 3.6V, DVSS= 0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{\text{CLK}}^{(1)}$	-	9	15	MHz
Hsync cycle	1/th	-	17.14	-	KHz
Vsync cycle	1/tv	-	59.94	-	Hz
Horizontal Signal					
Horizontal cycle	th	525	525	605	CLK
Horizontal display period	thd	480	480	480	CLK
Horizontal front porch	thf	2	2	82	CLK
Horizontal pulse width	thp ⁽²⁾	2	41	41	CLK
Horizontal back porch	thb ⁽²⁾	2	2	41	CLK
Vertical Signal					
Vertical cycle	tv	285	286	399	H ⁽¹⁾
Vertical display period	tvd	272	272	272	H ⁽¹⁾
Vertical front porch	tvf	1	2	227	H ⁽¹⁾
Vertical pulse width	tpv ⁽²⁾	1	10	11	H ⁽¹⁾
Vertical back porch	tvb ⁽²⁾	1	2	11	H ⁽¹⁾

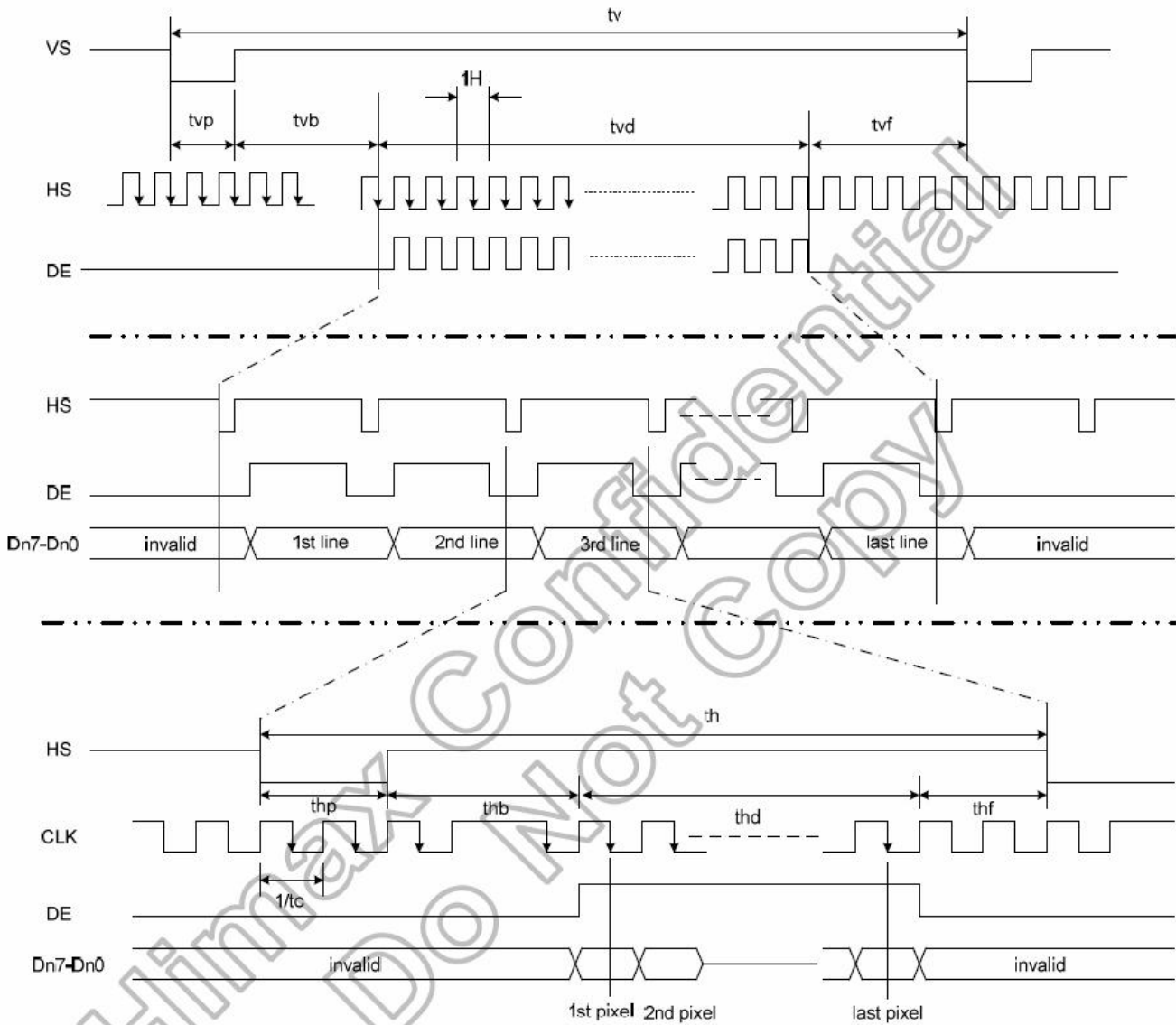
Note: (1) Unit: CLK=1/ f_{CLK} , H= th,

(2) It is necessary to keep $tpv+tvb=12$ and $thp+thb=43$ in sync mode. DE mode is unnecessary to keep it.

(480RGBx240, $T_A=25^{\circ}\text{C}$, VDDIO=1.8V to 3.6V, DVSS= 0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{\text{CLK}}^{(1)}$	-	9.6	15	MHz
Hsync cycle	1/th	-	15.72	-	KHz
Vsync cycle	1/tv	-	60	-	Hz
Horizontal Signal					
Horizontal cycle	th	525	612	-	CLK
Horizontal display period	thd	480	480	480	CLK
Horizontal front porch	thf	2	30	-	CLK
Horizontal pulse width	thp	2	46	-	CLK
Horizontal back porch	thb	2	56	-	CLK
Vertical Signal					
Vertical cycle	tv	-	262	275	H ⁽¹⁾
Vertical display period	tvd	-	240	-	H ⁽¹⁾
Vertical front porch	tvf	1	4	-	H ⁽¹⁾
Vertical pulse width	tpv	1	3	-	H ⁽¹⁾
Vertical back porch	tvb	1	15	-	H ⁽¹⁾

Note: (1) Unit: CLK=1/ f_{CLK} , H=th,



6.2.3 Serial RGB input timing requirement

(480RGBx272, $T_A=25^{\circ}\text{C}$, $V_{DDIO}=1.8\text{V}$ to 3.6V , $DVSS=0\text{V}$)

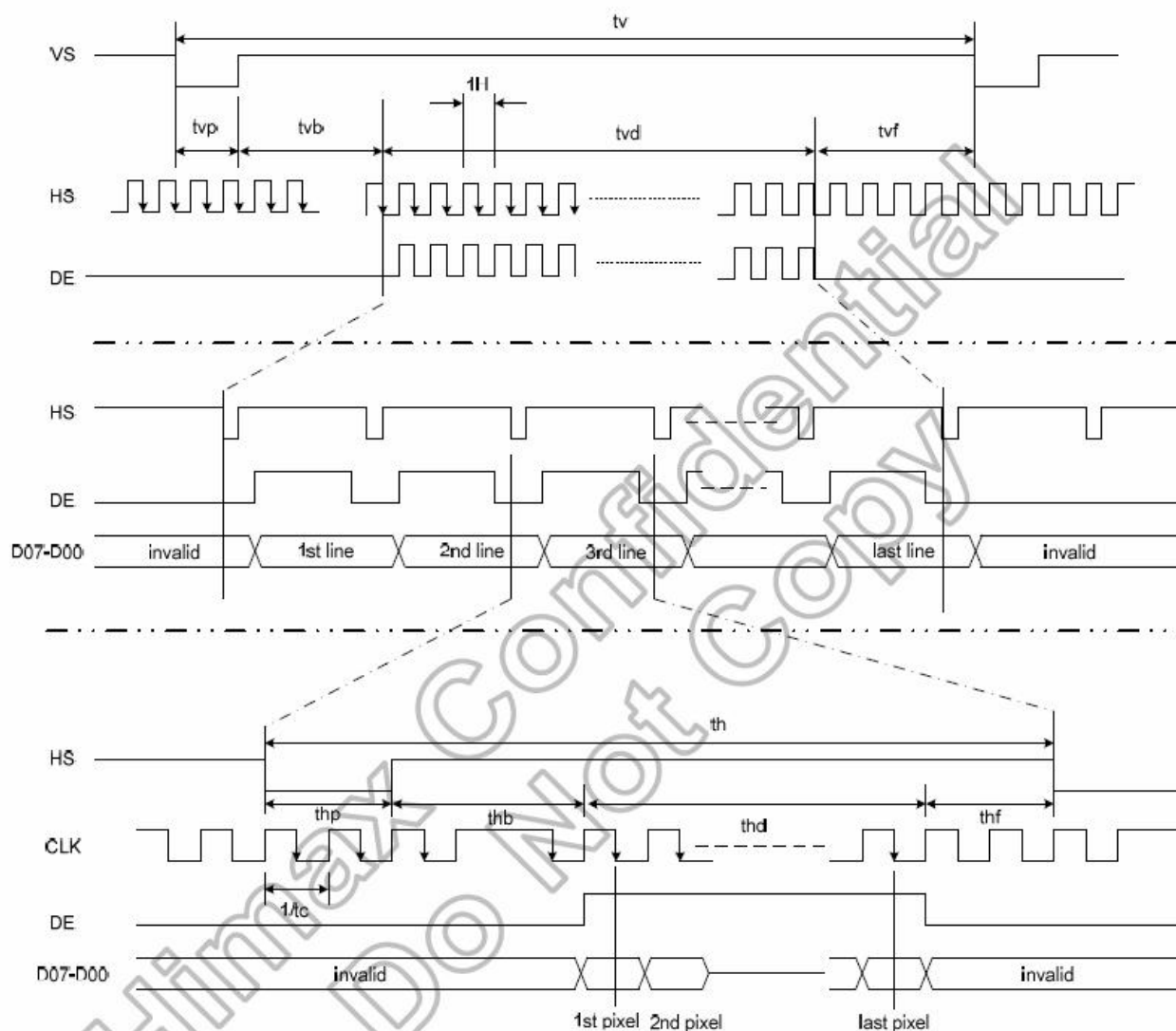
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{\text{CLK}}^{(1)}$	-	27	33	MHz
Hsync cycle	1/th	-	17.14	-	KHz
Vsync cycle	1/tv	-	59.94	-	Hz
Horizontal Signal					
Horizontal cycle	th	1575	1575	1815	CLK
Horizontal display period	thd	1440	1440	1440	CLK
Horizontal front porch	thf	6	6	246	CLK
Horizontal pulse width	thp	6	123	123	CLK
Horizontal back porch	thb	6	6	123	CLK
Vertical Signal					
Vertical cycle	tv	285	286	399	$H^{(1)}$
Vertical display period	tvd	272	272	272	$H^{(1)}$
Vertical front porch	tvf	1	2	227	$H^{(1)}$
Vertical pulse width	tvp	1	10	11	$H^{(1)}$
Vertical back porch	tvb	1	2	11	$H^{(1)}$

Note: (1) Unit: $\text{CLK}=1/f_{\text{CLK}}$, $H=\text{th}$

(480RGBx240, $T_A=25^{\circ}\text{C}$, $V_{DDIO}=1.8\text{V}$ to 3.6V , $DVSS=0\text{V}$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{\text{CLK}}^{(1)}$	-	28.8	33	MHz
Hsync cycle	1/th	-	15.72	-	KHz
Vsync cycle	1/tv	-	60	-	Hz
Horizontal Signal					
Horizontal cycle	th	1575	1836	-	CLK
Horizontal display period	thd	1440	1440	1440	CLK
Horizontal front porch	thf	6	90	-	CLK
Horizontal pulse width	thp	6	138	-	CLK
Horizontal back porch	thb	6	168	-	CLK
Vertical Signal					
Vertical cycle	tv	-	262	275	$H^{(1)}$
Vertical display period	tvd	-	240	-	$H^{(1)}$
Vertical front porch	tvf	1	4	-	$H^{(1)}$
Vertical pulse width	tvp	1	3	-	$H^{(1)}$
Vertical back porch	tvb	1	15	-	$H^{(1)}$

Note: (1) Unit: $\text{CLK}=1/f_{\text{CLK}}$, $H=\text{th}$



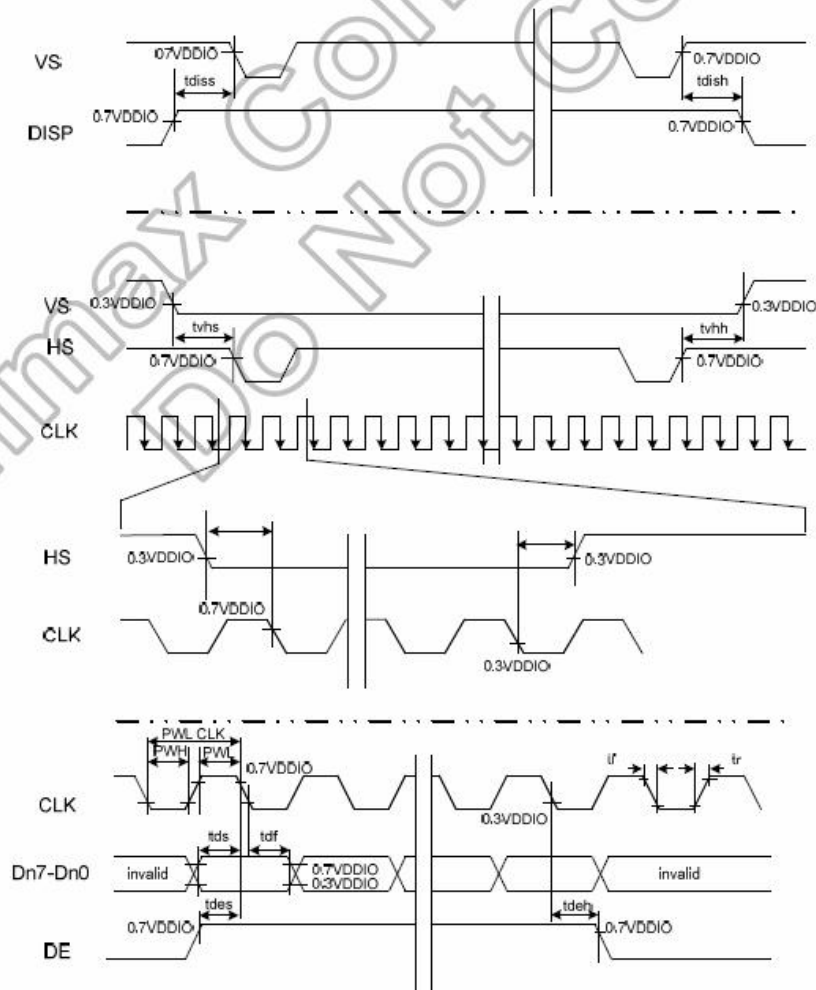
6.2.4 Input setup timing requirement

($T_A=25^\circ\text{C}$, $V_{DDIO}=1.8\text{V}$ to 3.6V , $DV_{SS}=0\text{V}$, $t_r^{(1)}=t_f^{(1)}=2\text{ns}$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DISP setup time	t_{diss}	10	-	-	ns
DISP hold time	t_{dish}	10	-	-	ns
Clock period	$PW_{CLK}^{(2)}$	66.7	-	-	ns
Clock pulse high period	$PWH^{(2)}$	26.7	-	-	ns
Clock pulse low period	$PWL^{(2)}$	26.7	-	-	ns
Hsync setup time	t_{hs}	10	-	-	ns
Hsync hold time	t_{hh}	10	-	-	ns
Data setup time	t_{ds}	10	-	-	ns
Data hold time	t_{dh}	10	-	-	ns
DE setup time	t_{des}	10	-	-	ns
DE hold time	t_{deh}	10	-	-	ns
Vsync setup time	t_{vhs}	10	-	-	ns
Vsync hold time	t_{vhh}	10	-	-	ns

Note: (1) t_r , t_f is defined 10% to 90% of signal amplitude.

(2) For parallel interface, maximum clock frequency is 15MHz.



7. Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	20	-	ms	FIG.1	Note4
Contrast Ratio		CR		350	500	-	-	FIG.2	Note1
Surface luminance		LV	$\theta = 0^\circ$	-	500	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	$\theta = 0^\circ$	-	80	-	%	FIG.2	Note3
NTSC		-	$\theta = 0^\circ$	-	50	-	%	FIG.2	Note5
Viewing angle		θ_T	Center CR ≥ 10	-	65	-	deg	FIG.3	Note6
		θ_B		-	55	-	deg	FIG.3	
		θ_L		-	65	-	deg	FIG.3	
		θ_R		-	65	-	deg	FIG.3	
Chromaticity	Red	R _X	$\theta = 0^\circ$ $\phi = 0^\circ$ Ta=25°	TBD	TBD	TBD	-	FIG.2 CIE1931	Note5
		R _Y		TBD	TBD	TBD	-		
	Green	G _X		TBD	TBD	TBD	-		
		G _Y		TBD	TBD	TBD	-		
	Blue	B _X		TBD	TBD	TBD	-		
		B _Y		TBD	TBD	TBD	-		
	White	W _X		TBD	TBD	TBD	-		
		W _Y		TBD	TBD	TBD	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is based on TOPCON's BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

L_v = Average Surface Luminance with all white pixels ($P_1, P_2, P_3, \dots, P_n$)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels } (P_1, P_2, P_3, \dots, P_n)}{\text{Maximum surface luminance with all white pixels } (P_1, P_2, P_3, \dots, P_n)}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_r) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_f) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is based on Autronic-Melchers' s ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

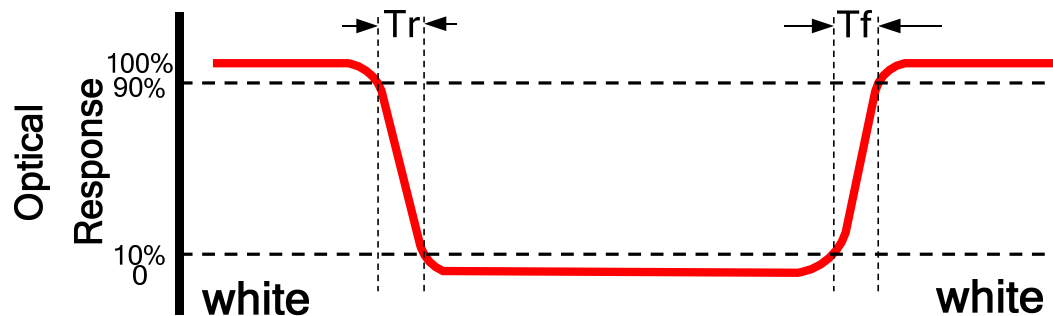


FIG.2. Measuring method for contrast ratio, surface luminance,

luminance uniformity, CIE (x,y) chromaticity

Size : $S \leq 5"$ (see Figure a) A : 5 mm B : 5 mm

H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

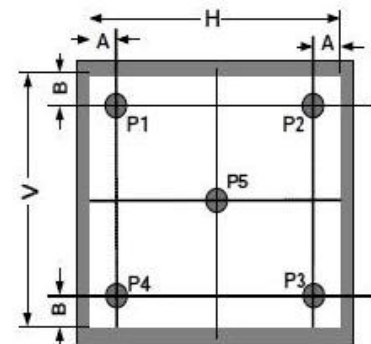


Figure a

Size : $5" < S \leq 12.3"$ (see Figure b) H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

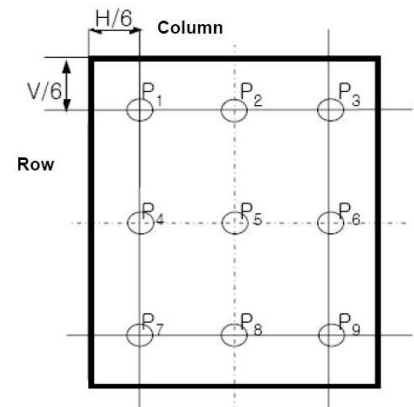


Figure b

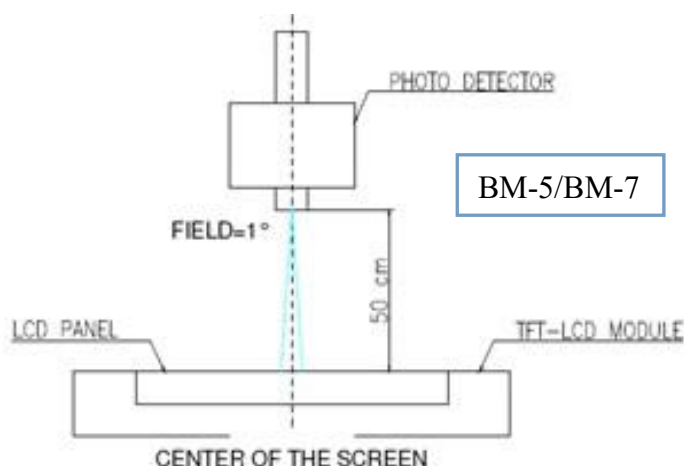
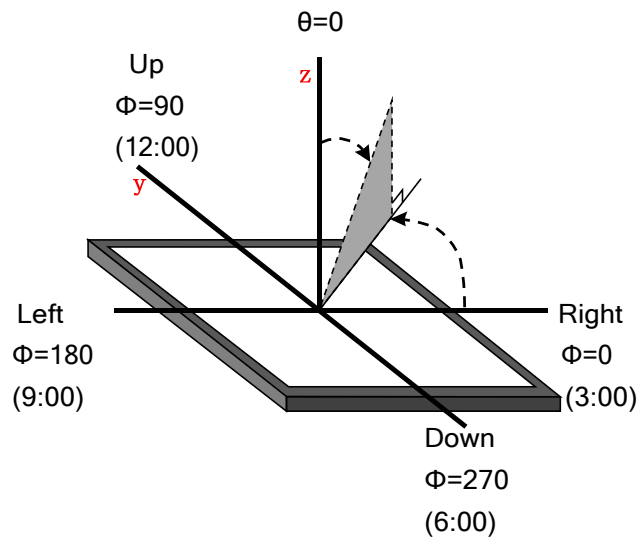


Figure c

FIG.3.The definition of viewing angle



8. Environmental / Reliability Tests

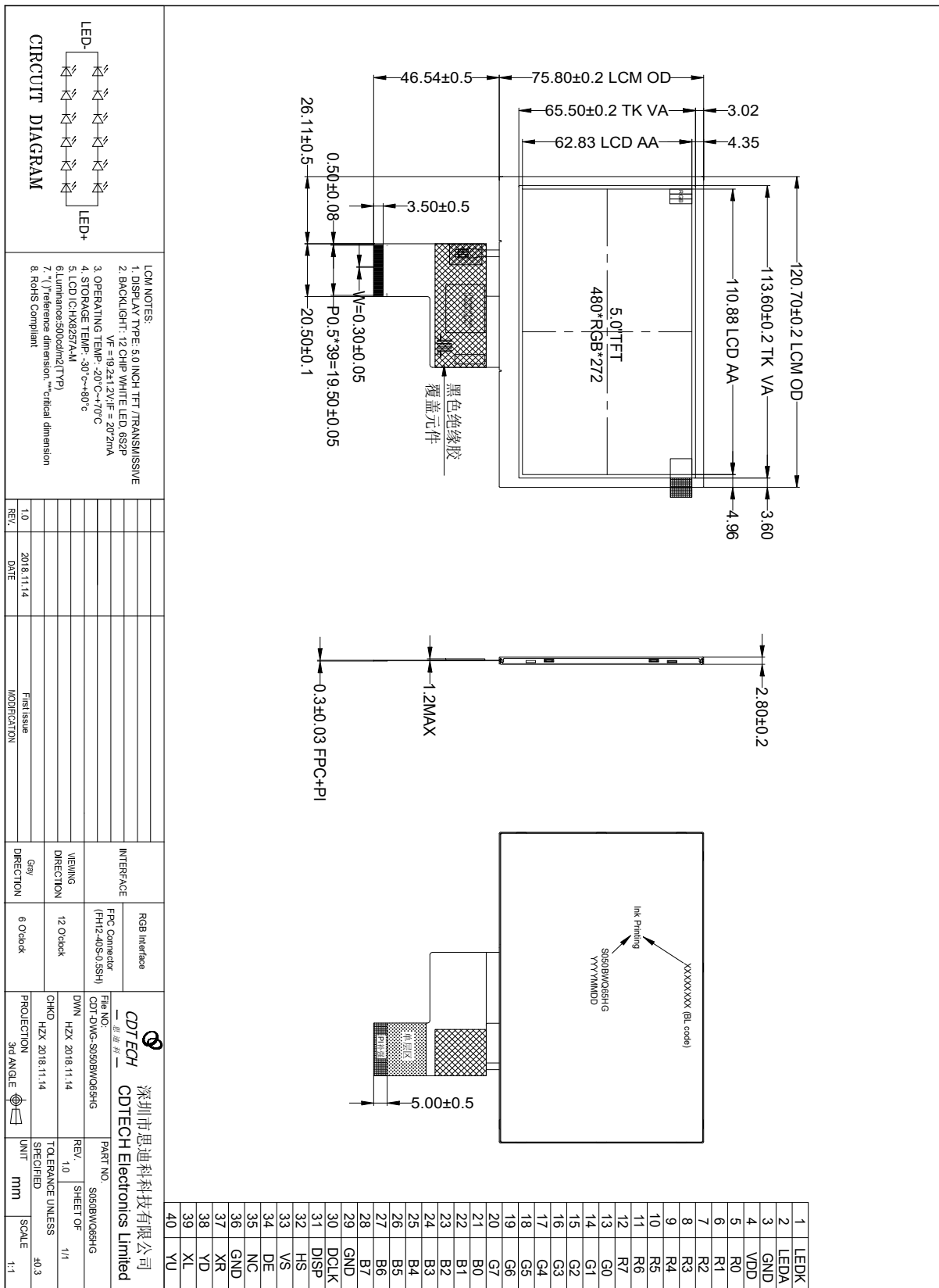
No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70°C, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20°C, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80°C, 96hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30°C, 96hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +70°C, 90% RH max,120 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20°C 30 min ~ +70°C 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Discharge (Operation) Static	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15°C ~ 35°C, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. Ts is the temperature of panel's surface.

2. Ta is the ambient temperature of sample.

3. The size of sample is 5pcs.

9. Mechanical Drawing



10. Packing

Packing Method

TBD

11. Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.