

CDTech(H.K.)Electronics Limited

Product Specification

Model Name	S024HQ36EN
Description	TFT LCD Module 2.4" QVGA 240(RGB)x320 Dots
Date	2018/8/17
Version	1.0

Approved by/Date	Check by/Date	Prepared by/Date
	ZHP 2018/8/17	Yigui.Han 2018/8/17

Customer Approval	
Date	

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2018/8/17	First Release.	Yigui.Han

2. General Specifications

Feature		Spec
Characteristics	Size	2.4 inch
	Resolution	240(horizontal)*320(Vertical)
	Interface	MCU8/16 bit OR RGB 18bit
	Connect type	Connector
	Display Colors	262K
	Technology type	a-Si
	Pixel pitch (mm)	0.153*0.153
	Pixel Configuration	R.G.B.-Stripe
	Display Mode	Normally White
	Driver IC	ILI9341
	Viewing Direction	6 O' clock
	Gray Inversion Direction	12 O'clock
Mechanical	LCM (W x H x D) (mm)	42.72*60.26*2.20
	Active Area(mm)	36.72*48.96
	Weight (g)	TBD
	LED Numbers	4 LEDs

Note 1: Requirements on Environmental Protection: RoHs

Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

LCD PIN-MAP

PIN NO.	PIN NAME	DESCRIPTION																																										
1	VCI	Power supply.																																										
2	IOVCC	Digital power supply.																																										
3	IM0	<table><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr></table>	1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]	1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]	1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]	1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]	1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out		1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out	
1	0		0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]																																					
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4	IM3																																											
5	IM2																																											
6	IM1																																											
7	RESET	Reset signal input terminal																																										
8	VSYNC	Vertical Sync signal																																										
9	HSYNC	Horizontal Sync signal																																										
10	DOTCLK	Dot clock signal.																																										
11	ENABLE	Data Enable																																										
12~29	DB17~DB0	DATA BUS.																																										
30	SDO	Serial output signal.																																										
31	SDI	Serial input signal.																																										
32	RD	Read signal																																										
33	WR/SCK	Write signal/ Serial Clock.																																										
34	RS	Data or Command select																																										
35	CS	Chip select																																										
36	GND	System Ground																																										
37	LEDA	LED Anode.																																										
38	LEDK1	LED Cathode.																																										
39	LEDK2	LED Cathode.																																										
40	NC	-																																										
41	NC	-																																										
42	NC	-																																										
43	NC	-																																										
44	NC	-																																										
45	NC	-																																										

4. Absolute Maximum Rating

Driving TFT LCD Panel

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V_{CC}	2.5	4.8	V	
Input Voltage	IOVCC	1.65	3.3	V	
Operating Temperature	T_{OPR}	-20	70	°C	
Storage Temperature	T_{STG}	-30	80	°C	

5. Timing characteristics

5.1 ELECTRICAL CHARACTERISTICS

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Analog Supply Voltage	V_{CC}	2.5	2.8	3.3	V	
Logic Signal Input /Output Voltage	IOVCC	1.65	1.8	3.3	V	
Input Signal Voltage	Low Level	V_{IL}	VSS	-	0.3x IOVCC	V
	High Level	V_{IH}	0.7x IOVCC	-	IOVCC	V
TFT Common Electrode	V_{COMH}	2.5	-	5	V	
TFT Gate ON Voltage	V_{GH}	10	-	16	V	
TFT Gate ON Voltage	V_{GL}	-10	-	-5	V	

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	
Forward Voltage	V_F	23.2	24	24.8	V	
Backlight Power consumption	W_{BL}	-	0.48	-		
LED Lifetime		-	25000	-	Hrs	

Note 1: Each LED: $I_F = 20 \text{ mA}$, $V_F = 6.2 \pm 0.2 \text{ V}$.

Note 2: Optical performance should be evaluated at $T_a = 25^\circ\text{C}$ only.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

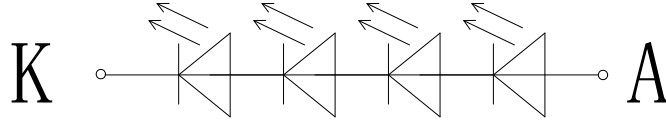
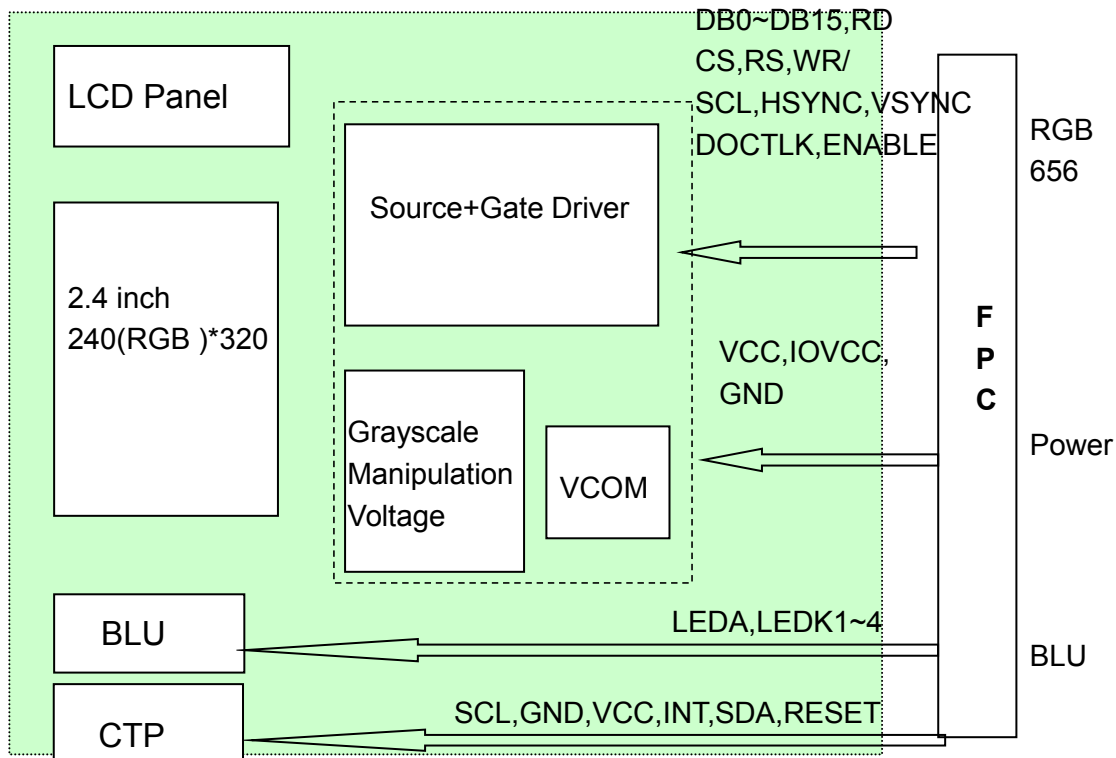


Figure: LED connection of backlight(Constant Current)

5.3 Block Diagram



6. Interface Timing

6.1 DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.3	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.3	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		$V_{CI} + 0.5$	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM} + 0.5$	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
$\Delta VLCD63$	Source voltage variation		-2		2	%
V _{OH1}	Logic High Output Voltage	I _{out} = -100 μ A	0.9*VDDIO	-	VDDIO	V
V _{OL1}	Logic Low Output Voltage	I _{out} = 100 μ A	0	-	0.1*VDDIO	V
V _{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V _{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I _{OH}	Logic High Output Current Source	V _{out} = V _{DDIO} - 0.4V	50	-	-	μ A
I _{OL}	Logic Low Output Current Drain	V _{out} = 0.4V	-	-	-50	μ A
I _{oz}	Logic Output Tri-state Current Drain Source		-1	-	1	μ A
I _{IL} /I _{IH}	Logic Input Current		-1	-	1	μ A

C _{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
R _{SON}	Source drivers output resistance		-	1	-	k Ω
R _{GON}	Gate drivers output resistance		-	5	-	k Ω
R _{CON}	Vcom output resistance		-	200	-	Ω
I _{dp} (262k)	Display current for 262k	V _{ddio} = 1.8V, V _{ci} = 2.8V, 5x/-5x booster ratio. Full color current consumption, without panel loading	I _{vdd}	-	150	300 μ A
			I _{vci}	-	2.5	8 mA
I _{dp} (8 color)	Display current for 8 color mode	Current consumption for 8 color partial display, without panel loading	I _{vdd}	-	120	300 μ A
			I _{vci}	-	1	5 mA
I _{slp}	Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode)	I _{vdd}	-	0.5	1 μ A
			I _{vci}	-	10	75 μ A

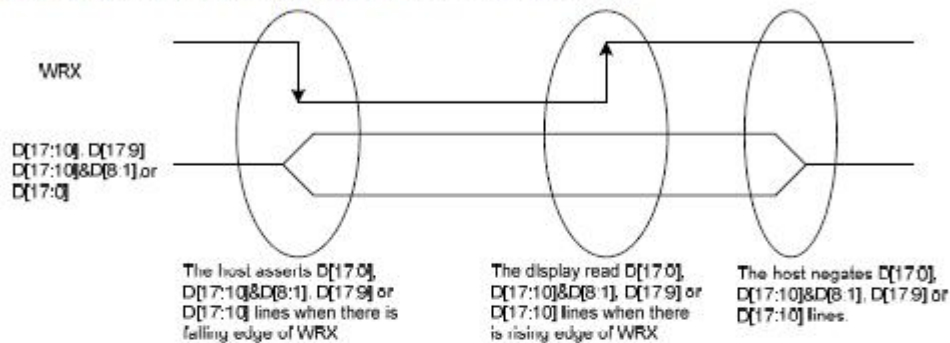
Remark: I_{vdd} = I_{vddio}

Note: The DC characteristic is base on only N-buffer or only P-buffer mode. (Refer to R3Fh command)

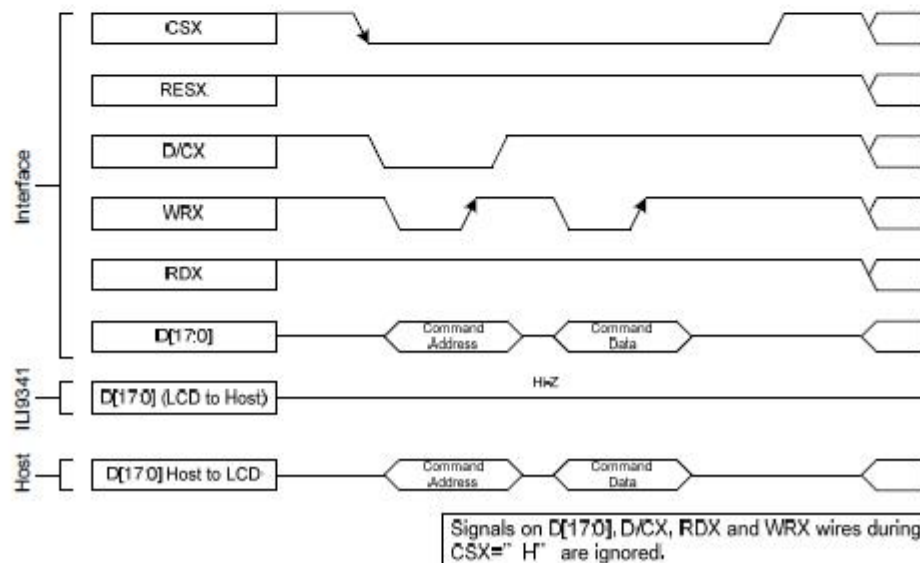
6.2 Timing

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

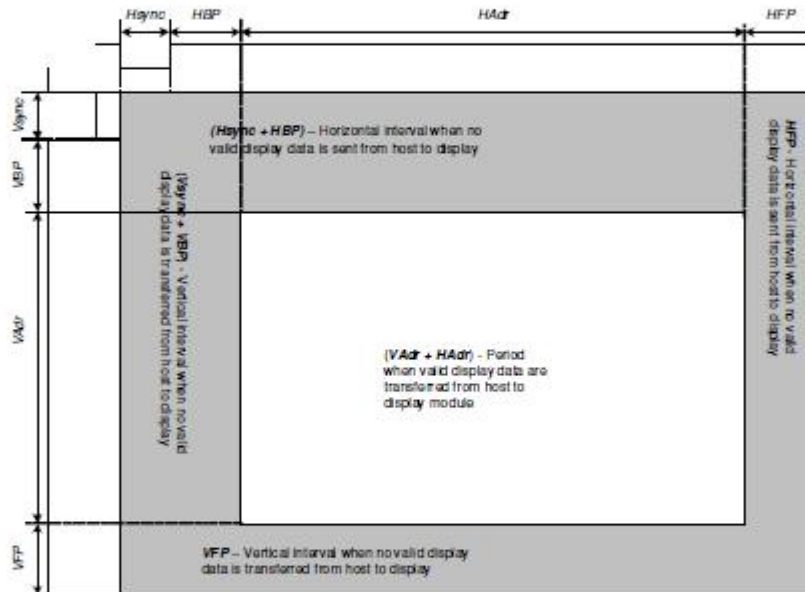
The following figure shows a write cycle for the 8080- Π MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)

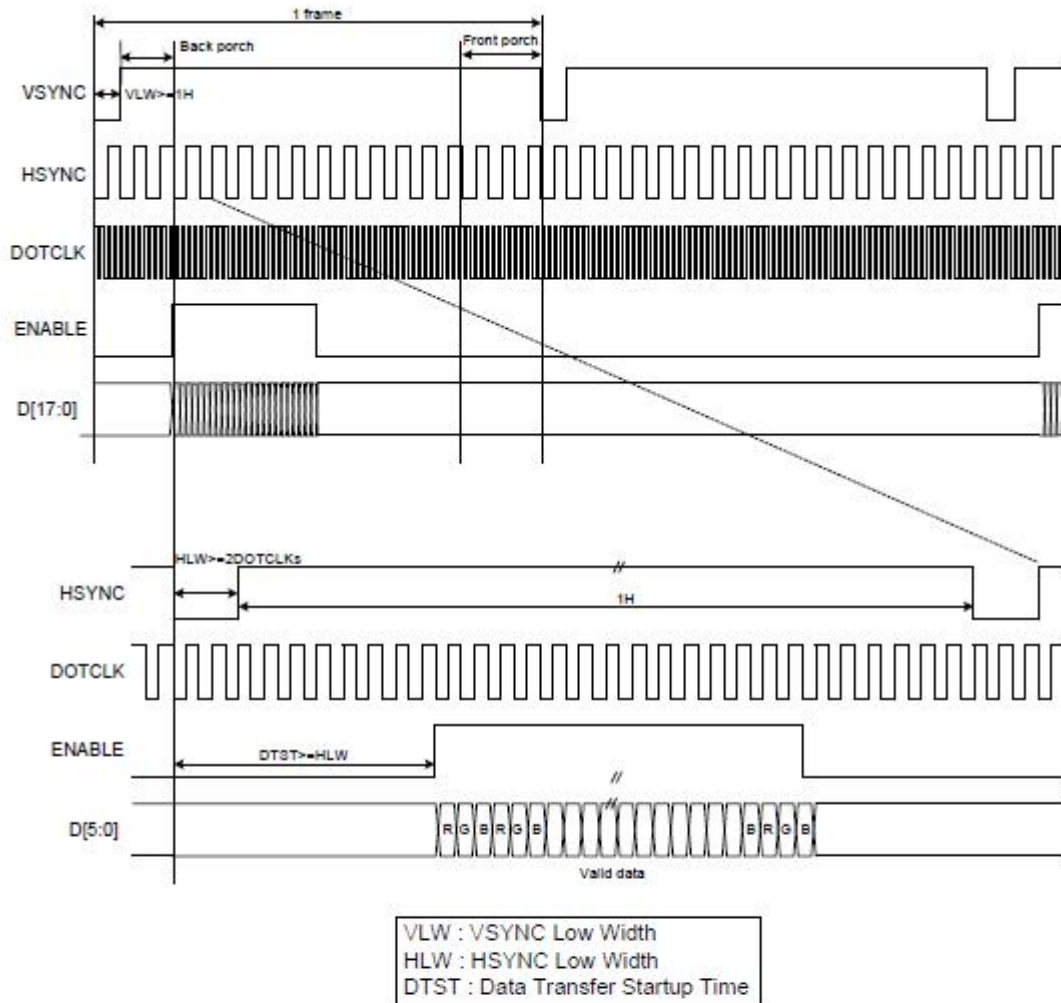
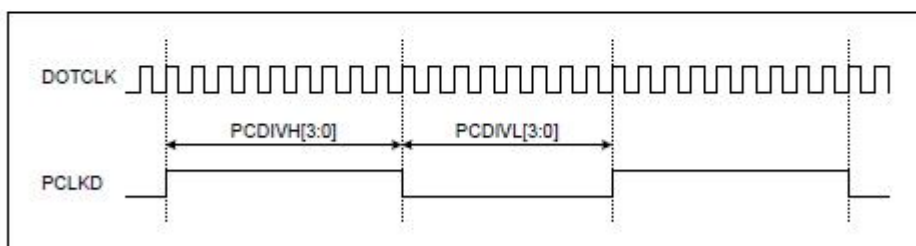


In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data is inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

The timing chart of 18-/16-bit RGB interface mode is shown as below.

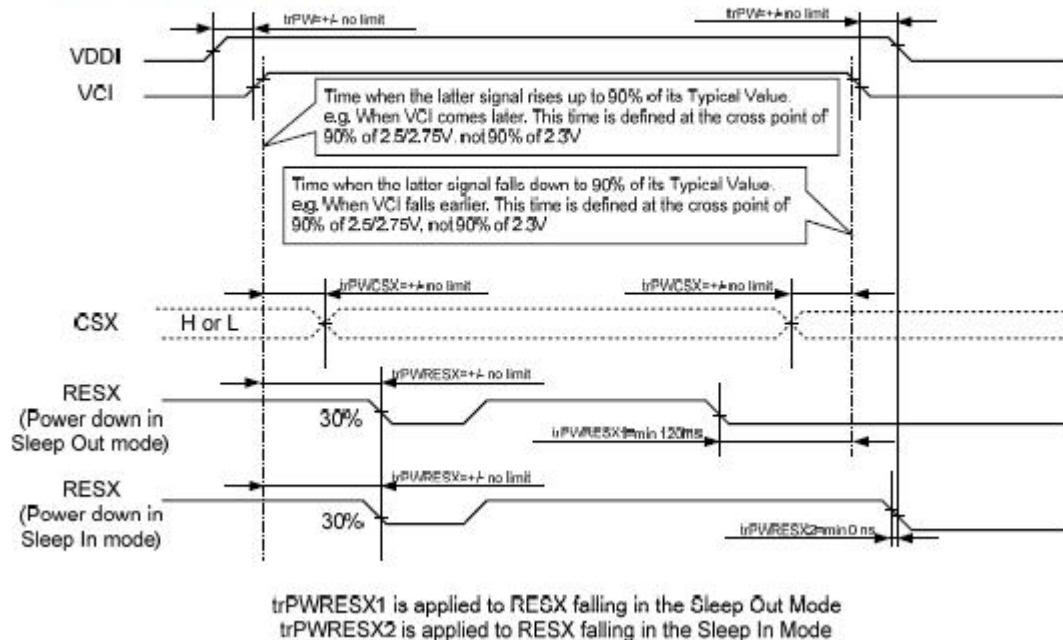


Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

6.3 Power ON/OFF Sequence

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



7. Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	45	65	ms	FIG.1	Note4
Contrast Ratio		CR		300	350	-	-	FIG.2	Note1
Surface luminance		LV	$\theta = 0^\circ$	-	800	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	$\theta = 0^\circ$	80	-	-	%	FIG.2	Note3
NTSC		-	$\theta = 0^\circ$	-	50	-	%	FIG.2	Note5
Viewing angle		θ	θ_T	-	55	-	deg	FIG.3	Note6
			θ_B	-	65	-	deg	FIG.3	
			θ_L	-	65	-	deg	FIG.3	
			θ_R	-	65	-	deg	FIG.3	
Chromaticity	Red	R _X	$\theta = 0^\circ$ $\phi = 0^\circ$ Ta=25°	TBD	TBD	TBD	-	FIG.2 CIE1931	Note5
		R _Y		TBD	TBD	TBD	-		
	Green	G _X		TBD	TBD	TBD	-		
		G _Y		TBD	TBD	TBD	-		
	Blue	B _X		TBD	TBD	TBD	-		
		B _Y		TBD	TBD	TBD	-		
	White	W _X		TBD	TBD	TBD	-		
		W _Y		TBD	TBD	TBD	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is based on TOPCON's BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

L_v = Average Surface Luminance with all white pixels($P_1, P_2, P_3, \dots, P_n$)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels } (P_1, P_2, P_3, \dots, P_n)}{\text{Maximum surface luminance with all white pixels } (P_1, P_2, P_3, \dots, P_n)}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_r) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_f) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P_5 . For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers’ s ConoScope or DMS series Instruments or compatible.

FIG.1. The definition of response Time

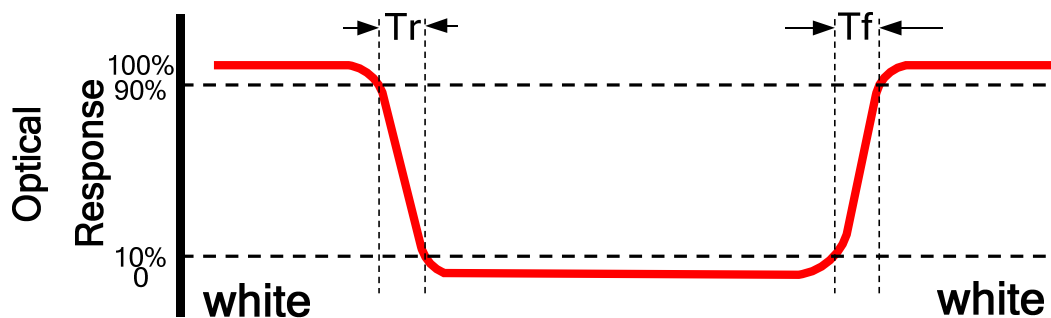


FIG.2. Measuring method for contrast ratio, surface luminance,

luminance uniformity, CIE (x,y) chromaticity

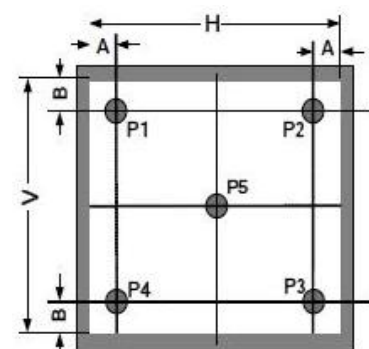
Size : $S \leq 5''$ (see Figure a) A : 5 mm B : 5 mm

H, V : Active area

Light spot size $\phi = 5\text{mm}$ (BM-5) or $\phi = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).



Size : $5'' < S \leq 12.3''$ (see Figure b) H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

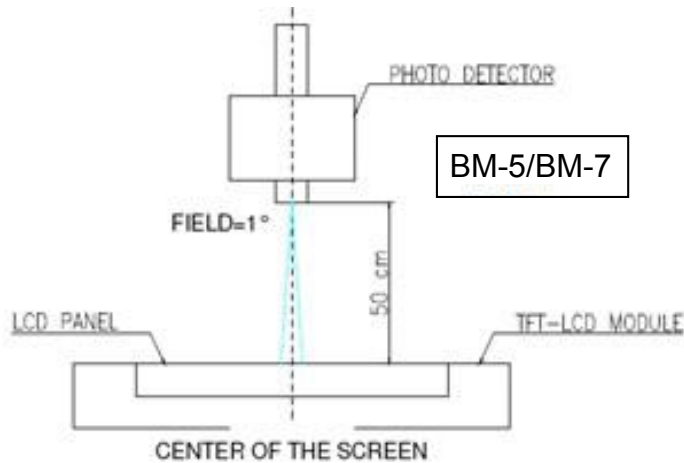


Figure c

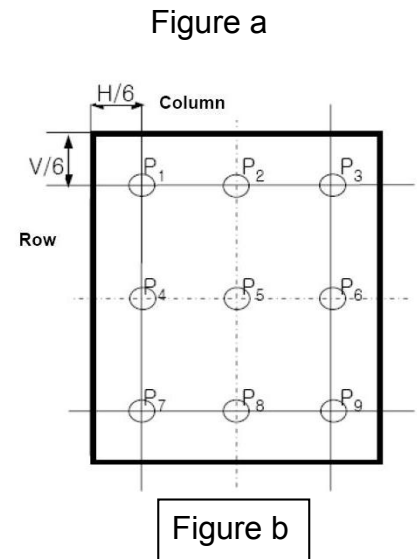
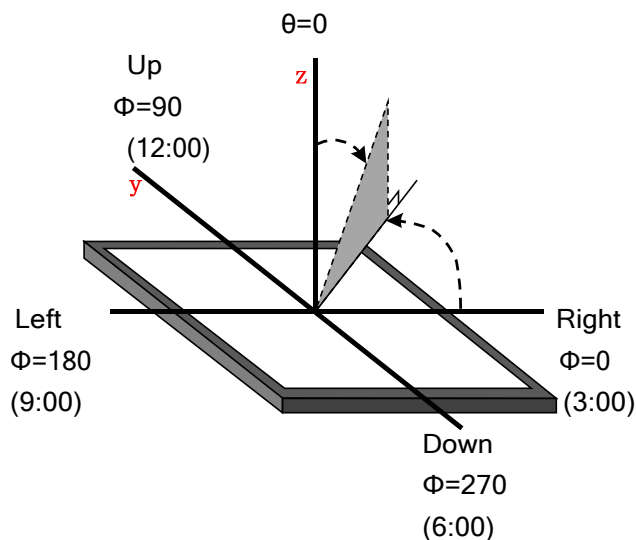


Figure a

Figure b

FIG.3.The definition of viewing angle

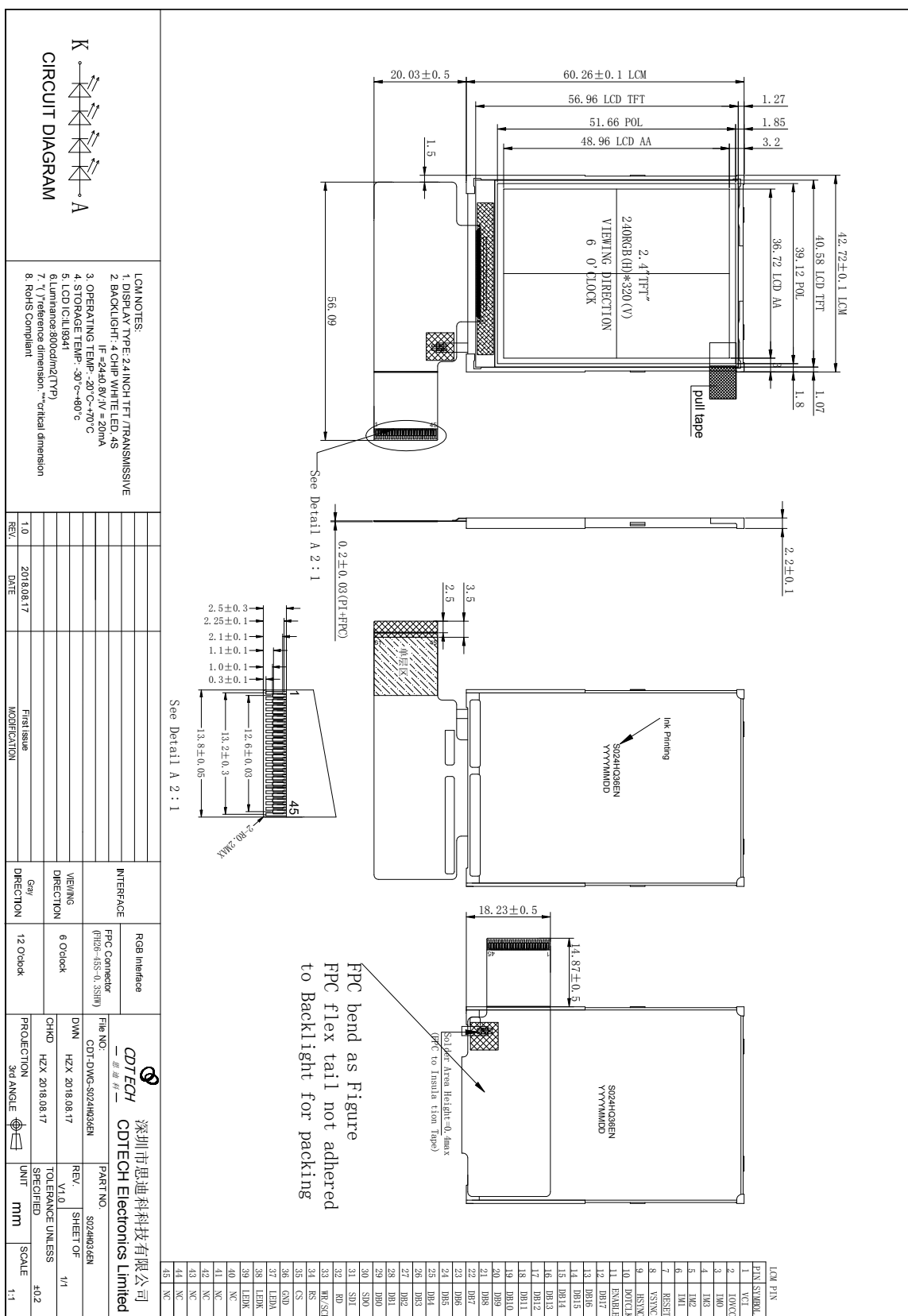


8. Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 96hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 96hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max,96 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20℃ 30 min ~ +60℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Discharge (Operation) Static	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

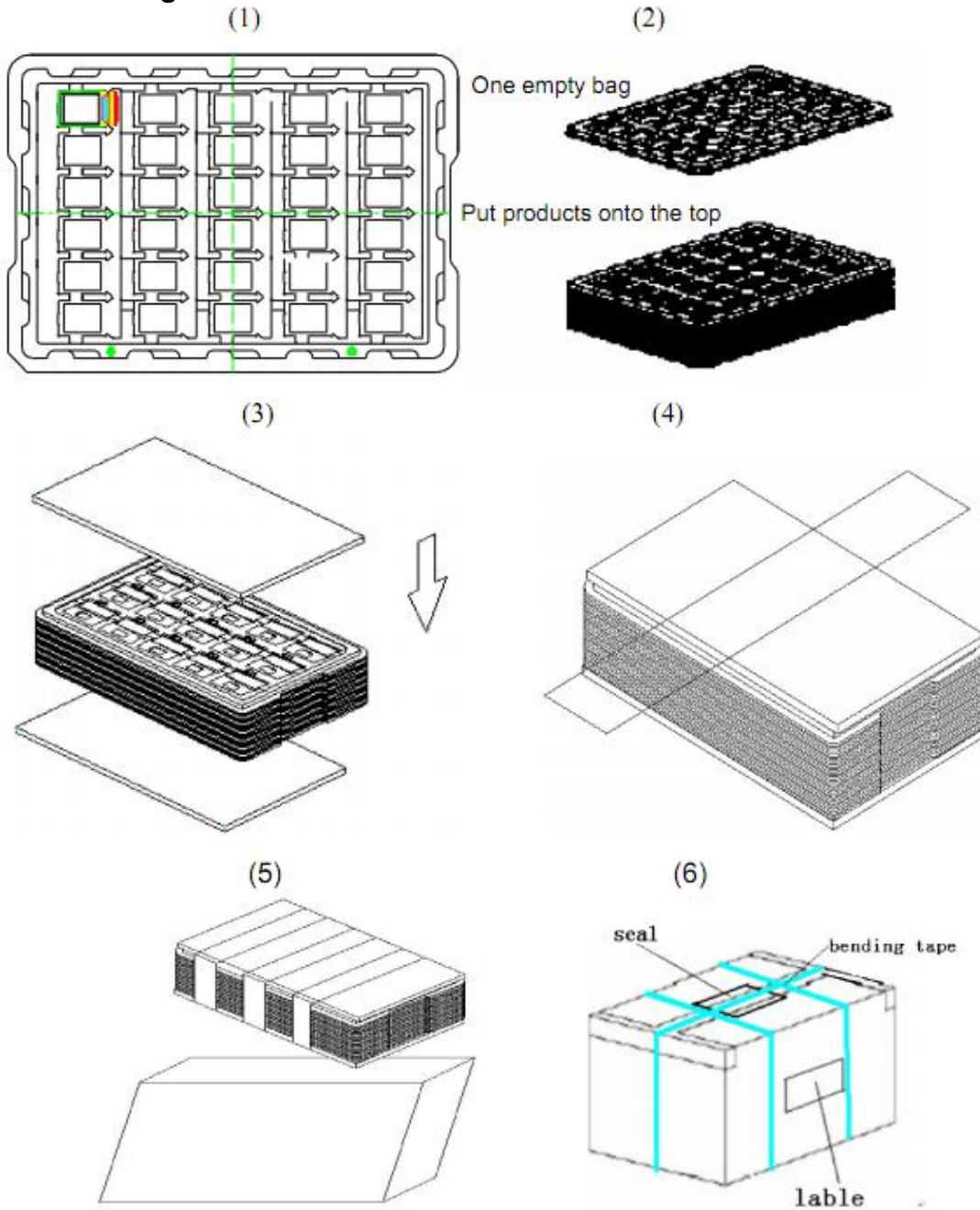
Note:1. Ts is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.
3. The size of sample is 5pcs.

9. Mechanical Drawing



10. Packing

Packing Method



1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

11. TFT-LCD Module Inspection Criteria

11.1 Scope

The incoming inspection standards shall be applied to TFT - LCD Modules (hereinafter Called "Modules") that supplied by CDTech Technology LTD.

11.2 Incoming Inspection

The customer shall inspect the modules within twenty calendar days of the delivery date (the “inspection period”) at its own cost. The result of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to The seller, If the results of the inspecting from buyer does not send to the seller within twenty Calendar days of the delivery date. The modules shall be regards as acceptance. Should the customer fail to notify the seller within the inspection period, the buyers Right to reject the modules shall be lapsed and the modules shall be deemed to have Been accepted by the buyer

11.3 Inspection Sampling

- 3.1. Lot size: Quantity per shipment lot per model
 - 3.2. Sampling type: Normal inspection, Single sampling
 - 3.3. Inspection level: II
 - 3.4. Sampling table: MIL-STD-105E
 - 3.5. Acceptable quality level (AQL)
- Major defect: AQL=0.65 Minor defect: AQL=1.00

11.4 Inspection Conditions

4.1 Ambient conditions:

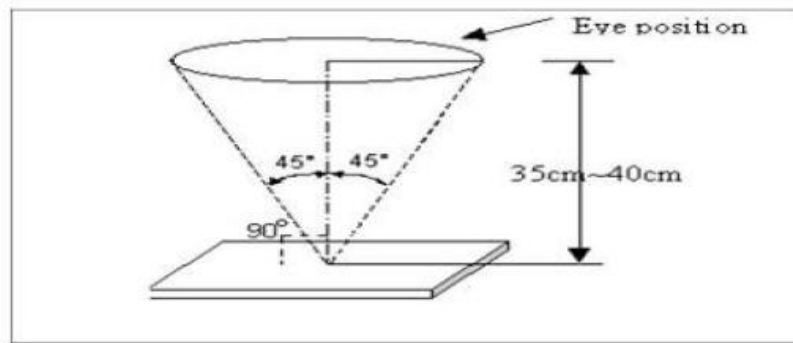
- a. Temperature: Room temperature $25 \pm 5^{\circ}\text{C}$
- b. Humidity: $(60 \pm 10) \% \text{RH}$
- c. Illumination: Single fluorescent lamp non-directive (300 to 700 Lux)

4.2 Viewing distance

The distance between the LCD and the inspector's eyes shall be at least $35 \pm 5 \text{ cm}$.

4.3 Viewing Angle

U/D: $45^{\circ} / 45^{\circ}$, L/R: $45^{\circ} / 45^{\circ}$



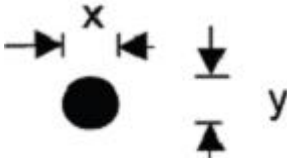
11.5 Inspection Criteria

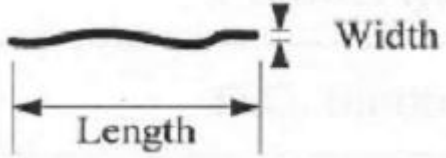
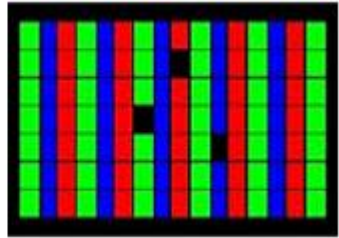
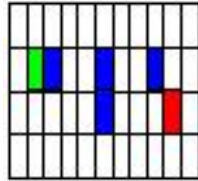
Defects are classified as major defects and minor defects according to the degree of Defectiveness defined herein.

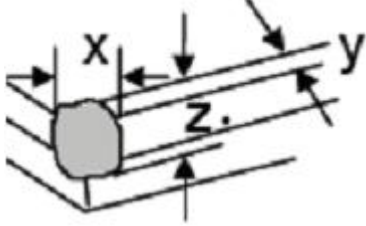
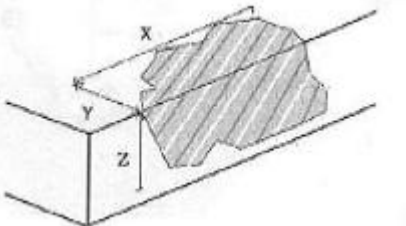
11.5.1 Major defect

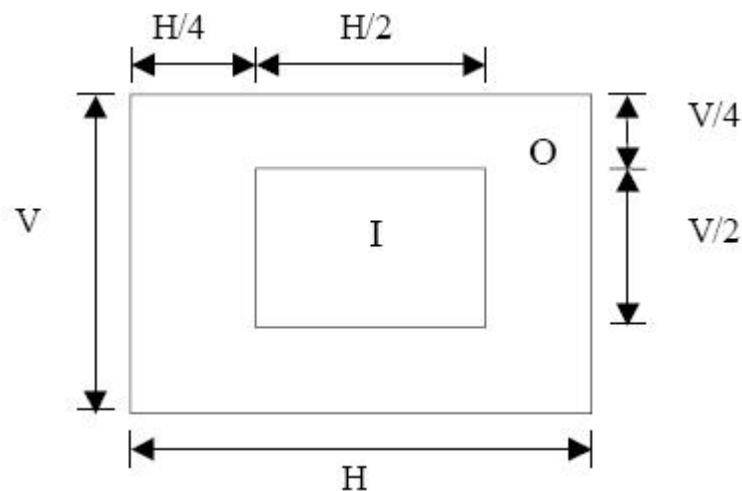
Item No	Items to be inspected	Inspection Standard
5.1.1	All functional defects	1) No display 2) Display abnormally 3) Short circuit 4) line defect
5.1.2	Missing	Missing function component
5.1.3	Crack	Glass Crack

11.5.2 Minor defect

Item No	Items to be inspected	Inspection standard	
5.2.1	Spot Defect Including Black spot White spot Pinhole Foreign particle Polarizer dirt	For dark/white spot is defined $\phi = (x+y) / 2$ 	
		Size ϕ (mm)	Acceptable Quantity
		$\phi \leq 0.05$	Ignore
		$0.05 < \phi \leq 0.15$	2
		$0.15 < \phi$	Not allowed
5.2.2	Polarizer dirt,	Size ϕ (mm)	Acceptable Quantity

	particle	$\phi \leq 0.15$	1			
		$\Phi > 0.15$	Not allowed			
5.2.3	Line Defect Including Black line White line Scratch	Define: 				
		Width(mm) Length(mm)		Acceptable Quantity		
		$W \leq 0.05$		Ignore		
		$0.05 < W \leq 0.1$ $L \leq 1.5$		1		
		$0.1 < W$, or $L > 1.5$		Not allowed		
5.2.4	Polarizer Dent/Bubble	Not allowed				
5.2.5	Electrical Dot Defect	Bright and Black dot define:  and   Two Adjacent Dot				
		Inspection pattern: Full white、Full black、Red、green and blue screens				
		Item		Acceptable Quantity		
				I	O	Note
		Black dot defect		1		(5mm≤Distance)
		Bright dot defect		1		
		Two Adjacent Dot		Not allow		

5.2.6	Glass defect	 <p>1. Corner Fragment:</p>	
		Size(mm)	Acceptable Quantity
		$X \leq 2\text{mm}$ $Y \leq 1\text{mm}$ $Z \leq T$	Ignore T: Glass thickness X: Length Y: Width Z: thickness
		<p>2. Side Fragment:</p> 	
		Size(mm)	Acceptable Quantity
		$X \leq 5.0\text{mm}$ $Y \leq 1\text{mm}$ $Z \leq T$	T: Glass thickness X: Length Y: Width Z: thickness



I area & O area

- Note:
- 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.
 - 2). The distance between two bright dot defects (red, green, blue, and white) should be larger than 15mm.
 - 3). The distance between black dot defects or black and bright dot defects should be more than 5mm apart.
 - 4). Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.

11.6 Mechanics specification

As for the outside dimension, weight of the modules, please refer to product specification
For more details

12. Precautions for Use of LCD modules

12.1 Handling Precautions

12.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

12.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

12.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

12.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

12.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

12.1.6. Do not attempt to disassemble the LCD Module.

12.1.7. If the logic circuit power is off, do not apply the input signals.

12.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

12.1.8.1. Be sure to ground the body when handling the LCD Modules.

12.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

12.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

12.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

12.2 Storage Precautions

12.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

12.2.2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

12.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

12.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.